A CAHNERS PUBLICATION

INTERNATIONAL EDITION NOVEMBER 23, 1989

EDN®

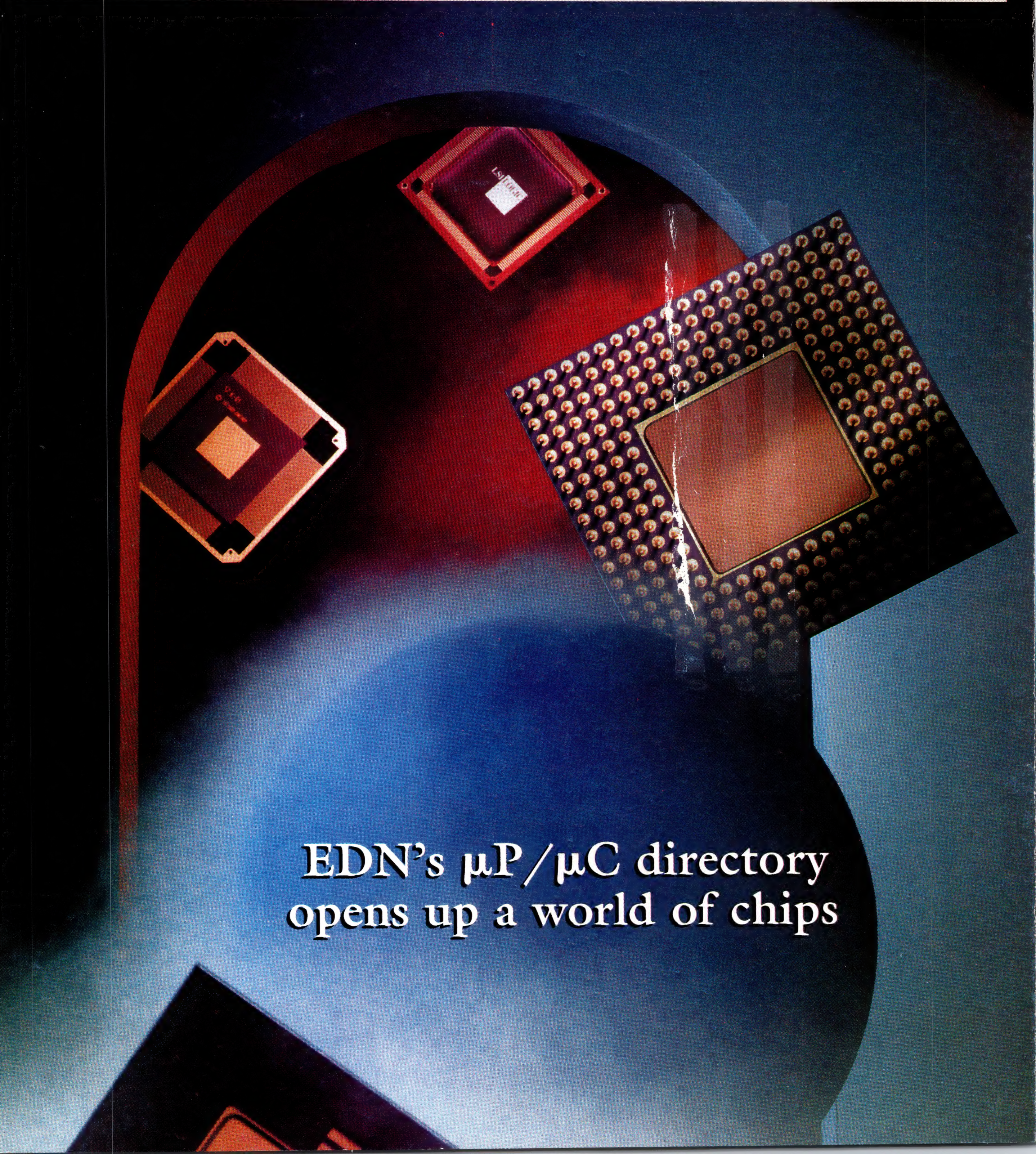
Designer's guide to resonant-mode supplies

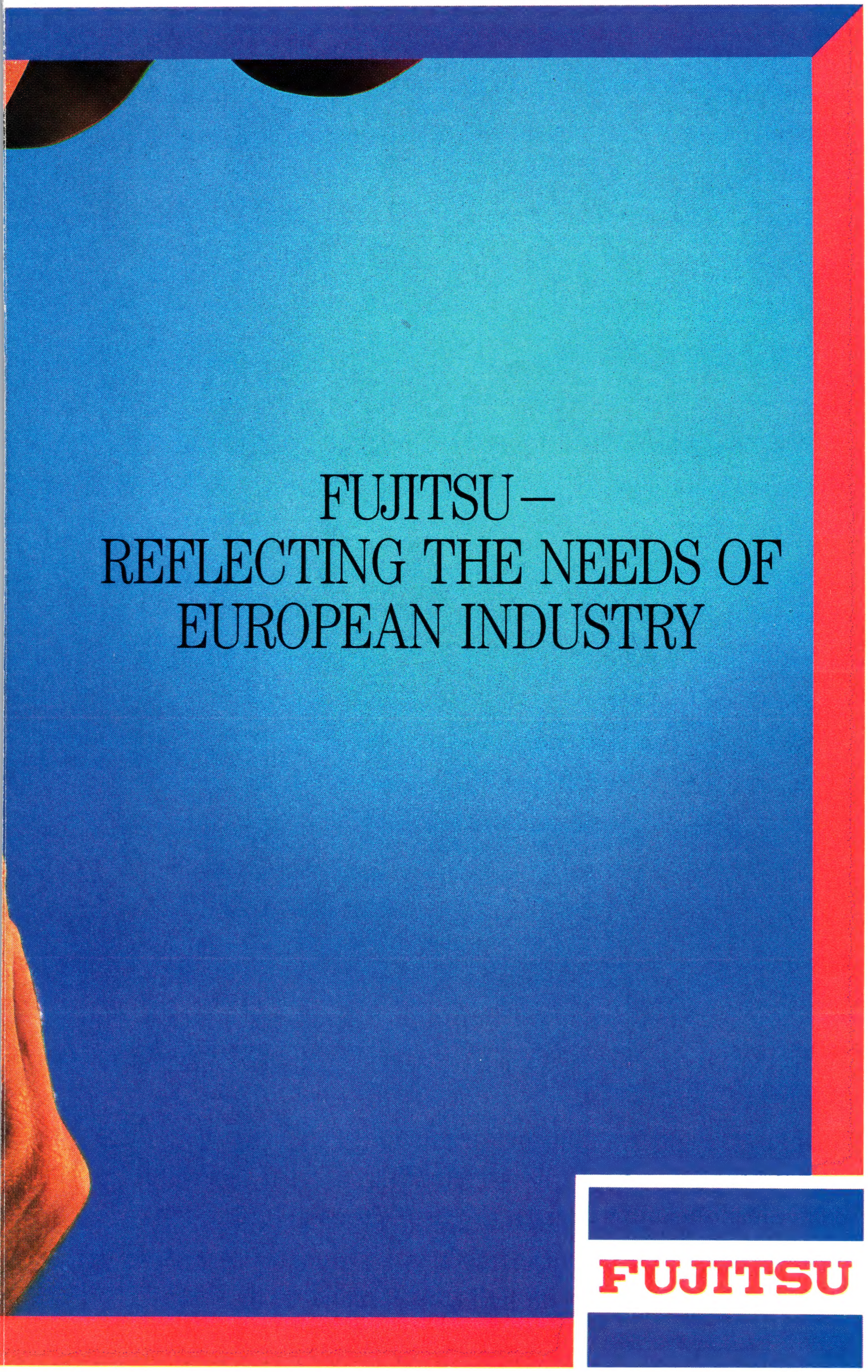
Algorithm facilitates image recognition

VXIbus product roundup

Verification testers ease ASIC development

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS





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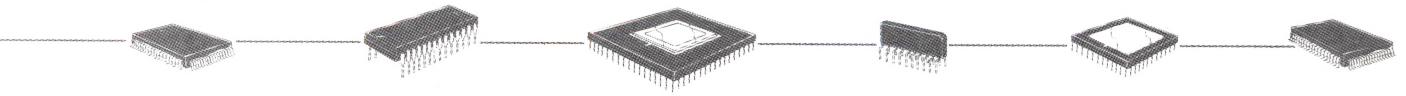

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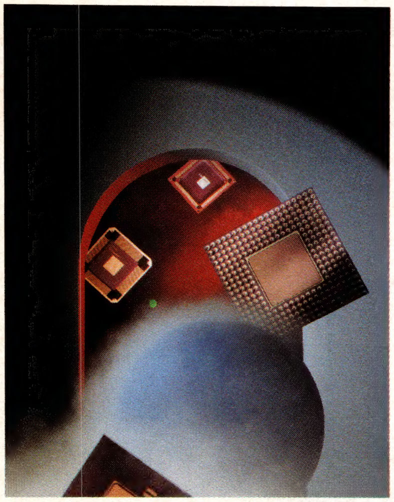
EDN Magazine Edition®

Volume 34, Number 24 November 23, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: ***A universe of chips opens up in EDN's 16th Annual μP/μC Chip Directory. Many vendors are beginning to realize that giving you a CPU with the right combination of peripherals provides you with the greatest benefit. See our Special Report on pg 92. (Photo courtesy LSI Logic; concept and photography by Imagination)***

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

VBPA ABP

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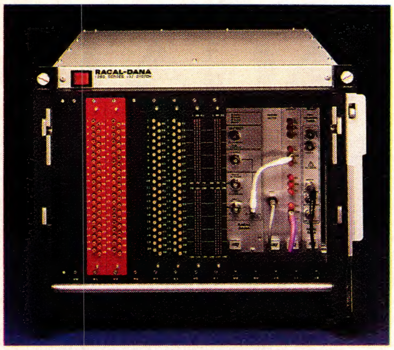
Continued from page 5

EDN Magazine Edition

November 23, 1989



EDN's first roundup of VXIbus *products lists 182 offerings. The number of products suggests that despite the newness of the modular-instrumentation standard, the standard is headed for success (pg 51).*

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

TECHNOLOGY UPDATES

Continued on page 9

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Continued from page 7

EDN Magazine Edition

November 23, 1989

NEW PRODUCTS

DEPARTMENTS

COMING ATTRACTIONS

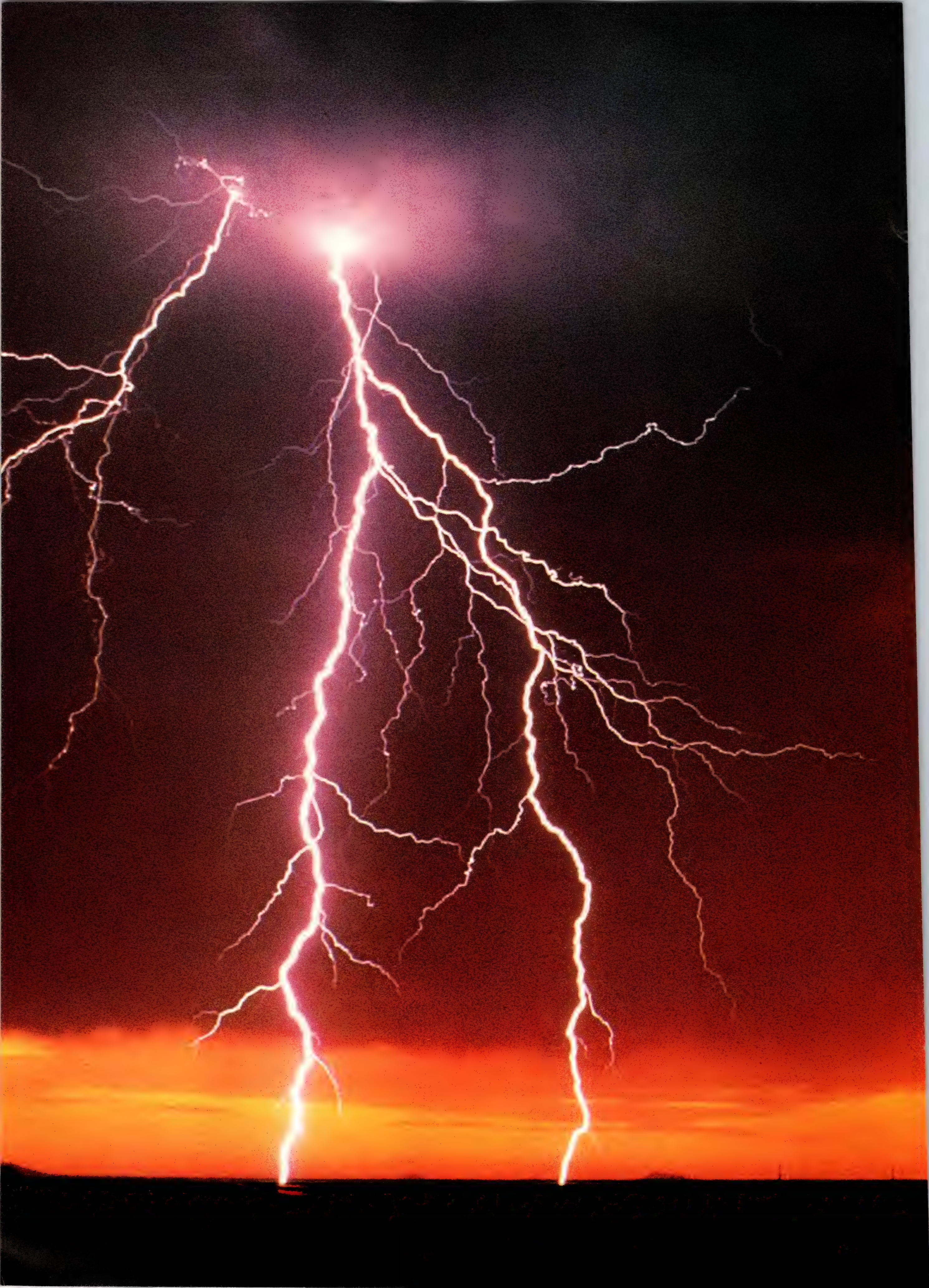
EDN's Product Showcase begins with the December 7, 1989, issue. Part 1 of the showcase will feature staff-written articles and product reviews of four key technology areas:

- Hardware and Interconnect Devices
- Integrated Circuits
- Power Supplies
- Software.

The December 21, 1989, issue follows with Part 2 of the showcase. This issue will feature coverage of four different technology areas of importance to EDN readers:

- Instruments
- Computers and Peripherals
- Computer-Aided Engineering
- Components.

Also, be sure to look for our regular departments in both issues.



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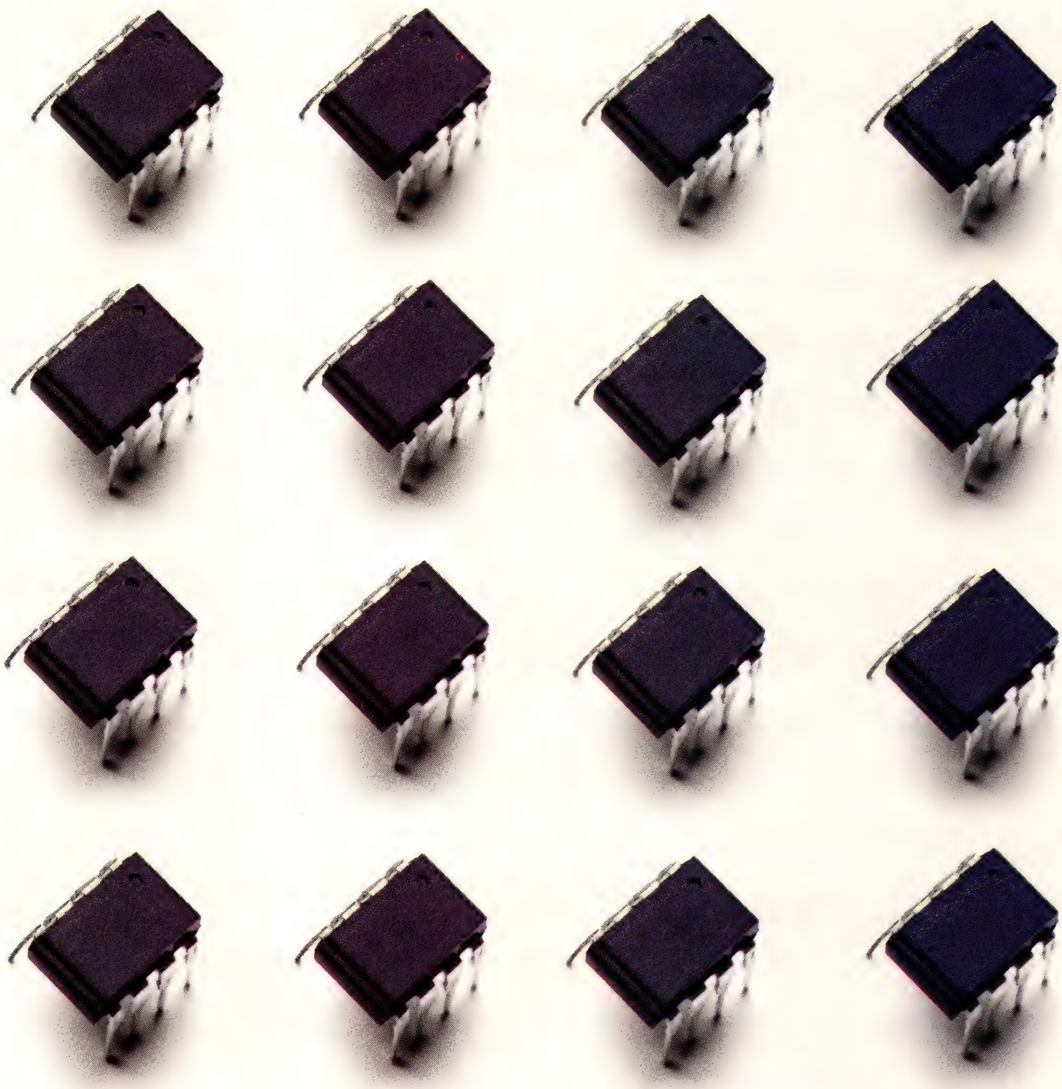

NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

DSO ACCEPTS 40-GHz-BANDWIDTH PLUG-IN

The CSA 803 communications signal analyzer from Tektronix Inc (Beaverton, OR, (800) 835-9433) physically resembles the 11800 DSO family that Tek introduced less than a year ago but incorporates trigger features not present in the 11800—including a prescaler that allows triggering on 10-GHz signals. Without the prescaler, triggering only extends to 2.5 GHz. In addition, the firmware includes several features useful in conjunction with "eye" diagrams—a tool widely used in characterizing noise and jitter in very wideband communications links, for example, fiber-optic networks. The unit constructs histograms and lets you create and edit templates on its touch-sensitive color screen. You can store the templates in nonvolatile RAM and use them to determine whether particular signals fall within or outside your spec. One of the sampling plug-ins offered with the unit has a 40-GHz bandwidth, and an optical-to-electrical converter plug-in is available for fiber-optic work. Prices start at $31,000.—Dan Strassberg

$495 SCHEMATIC PACKAGE INCLUDES 5000 DEVICE MODELS

Accel Technologies Inc (San Diego, CA, (619) 554-1000) now offers its $495 Tango-Schematic Series II package as a companion to its low-cost pc-board layout and autorouting products. The product supports hierarchical schematic design with an unlimited number of hierarchical levels and lets you create 99 schematic sheets per level. On-line, context-sensitive help is always available, and you can create parts on the fly using the integrated component-creation facility. However, the schematic-capture package includes a component library with 5000 device models, so you can probably start drawing schematics immediately instead of first creating the components you need. The standard parts library includes TTL, CMOS, and CMOS logic; µPs and peripherals; PLDs; linear ICs; discrete semiconductors; electromechanical components; and passive devices. Standard Engineering Data Co (Sedco) (Scotts Valley, CA, (408) 438-7885) created the parts library.

Tango-Schematic Series II can print schematics on a variety of plotters and printers and can emit the schematic in the PostScript format. In addition, the package generates net lists, bills of materials, part-usage reports, design statistics, hierarchy trees, component cross references, library contents reports, and parts locaters.
—Steven H Leibson

MICROCONTROLLERS RUN 5 MIPS

The PIC16C54 and PIC16C55 microcontrollers from Microchip Technology (Chandler, AZ, (602) 963-7373) are the first in a planned family of RISC-like CMOS microcontrollers. Their architecture includes an instruction pipeline and 32 general-purpose registers. The microcontrollers' op codes are 12 bits long and mix instructions and data. These 12 bits include all necessary operands or data, thus allowing each instruction to execute in a single instruction cycle. Running at a clock rate of 20 MHz, the devices execute 5 MIPS.

The controllers include EPROM, a counter/timer, a watchdog timer with its own oscillator, and bidirectional I/O lines. The 28-pin 16C55 has 21 I/O lines; the 18-pin 16C54 has 13 I/O lines. The devices are available in three speed grades—400 kHz, 4

MHz, and 20 MHz—thus letting you trade off power consumption and speed. Both company-produced and third-party development tools are available for the devices. The PIC16C54 and PIC16C55 are available in DIPs, SOICs, and plastic leaded-chip carriers; prices start at $2.40 (2500).—Richard A Quinnell

BIPOLAR VIDEO DAC REACHES 500 MHz

The CXA1236Q 500-MHz single video DAC from Sony Corp (Cypress, CA, (714) 229-4183) is a bipolar 8-bit video DAC. Previously, 500-MHz video DACs were available only in GaAs. The monolithic part's supply voltage can range from −4.2 to −5.5V with a power dissipation of 930 mW. The two multiplexed 8-bit inputs are ECL 100K and 10K compatible, and the video output is RS-343A compatible. Sony will announce pricing and begin offering samples in December.—Margery Conner

COMDEX PRODUCTS SPAN COMPUTER AND PERIPHERAL PRODUCTS

3M (St Paul, MN, (612) 733-1110) has developed a prototype drive that implements a new QIC (quarter inch cartridge) standard, QIC-1350, which specifies a tape drive that stores 1.35G bytes. The company has no plan to manufacture the new drive. Instead, it plans to license the technology to OEM manufacturers of QIC tape drives. The drive uses a new cartridge developed by 3M that contains 750 ft of 900-Oe tape. The company has signed several undisclosed licensees and expects a drive based on the technology to be available sometime in 1990 at an OEM price of around $750. The drive stores data on 30 tracks at a density of 38750 flux transitions/sec. The drive transfers data at 597k bytes/sec—three times faster than 1G-byte digital-audio-tape drives. The drive also includes downward compatibility with 120M-, 150M-, and 320M-byte QIC drives.

Also at Comdex, Advanced Logic Research (Irvine, CA, (714) 581-6770) announced a 33-MHz version of its MicroFlex 80386, Micro Channel Architecture computer. The Model 70 employs the company's FlexCache external cache, which consists of 128k bytes of RAM organized with a 64-bit data path. Standard features include VGA graphics and a 70M-byte ESDI disk drive for the $5795 list price. The computer comes with 2M bytes of RAM, which you can expand to 64M bytes. You can also specify the system in a tower configuration with larger disk drives and with an intelligent graphics controller that supports a 1024×768-pixel resolution and 256 colors.

Other Comdex product announcements included 2½- and 3½-in. disk drives from Conner Peripherals (San Jose, CA, (408) 433-3340) that address applications ranging from notebook-to desktop-size systems. The CP-2024 2½-in. drive, for example, stores 21.4M bytes and offers an average seek time of 23 msec. The $550 drive can withstand a 100g shock (nonoperating), weighs 5.5 oz, and requires 1.5W in idle mode. The company also introduced the $450, 21.4M-byte CP-4024 and $550, 42.6M-byte CP-4044 3½-in. drives. These drives match the 5.15-in. depth of low-profile floppy-disk drives and feature average seek times of less than 29 msec. Finally, the company introduced the 120M-byte, 1-in.-high, 3½-in. CP-30100 drive, which costs $750. This drive offers an average seek time of less than 19 msec and consumes 2.5W.—Maury Wright

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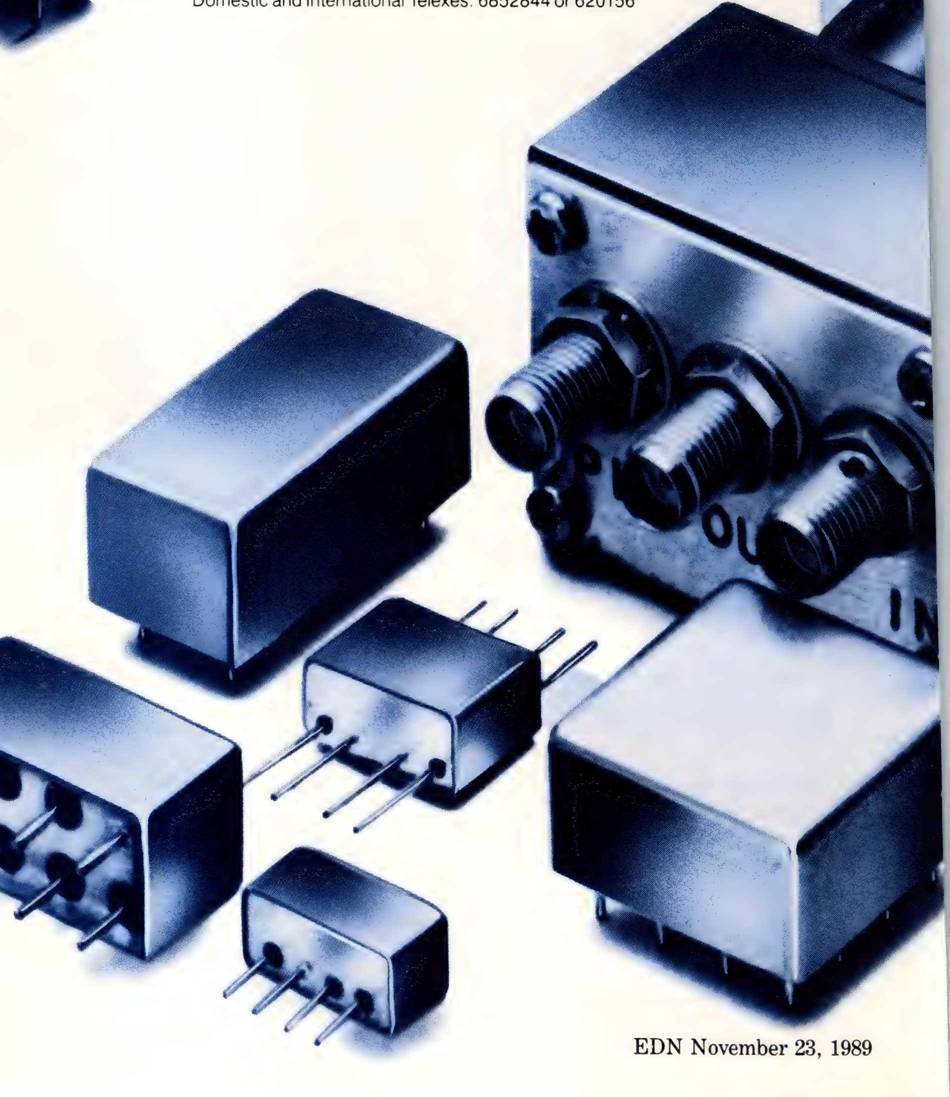

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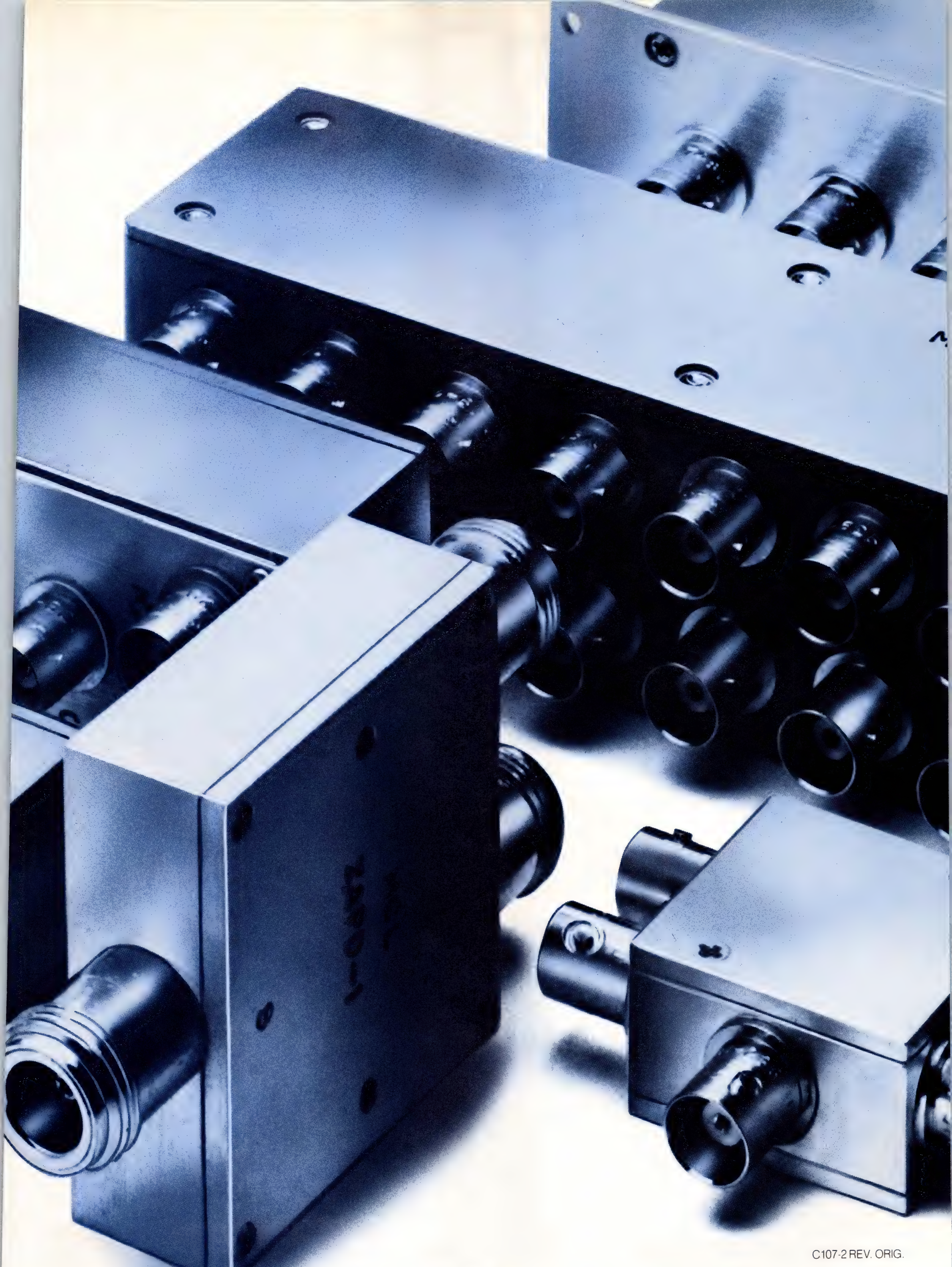


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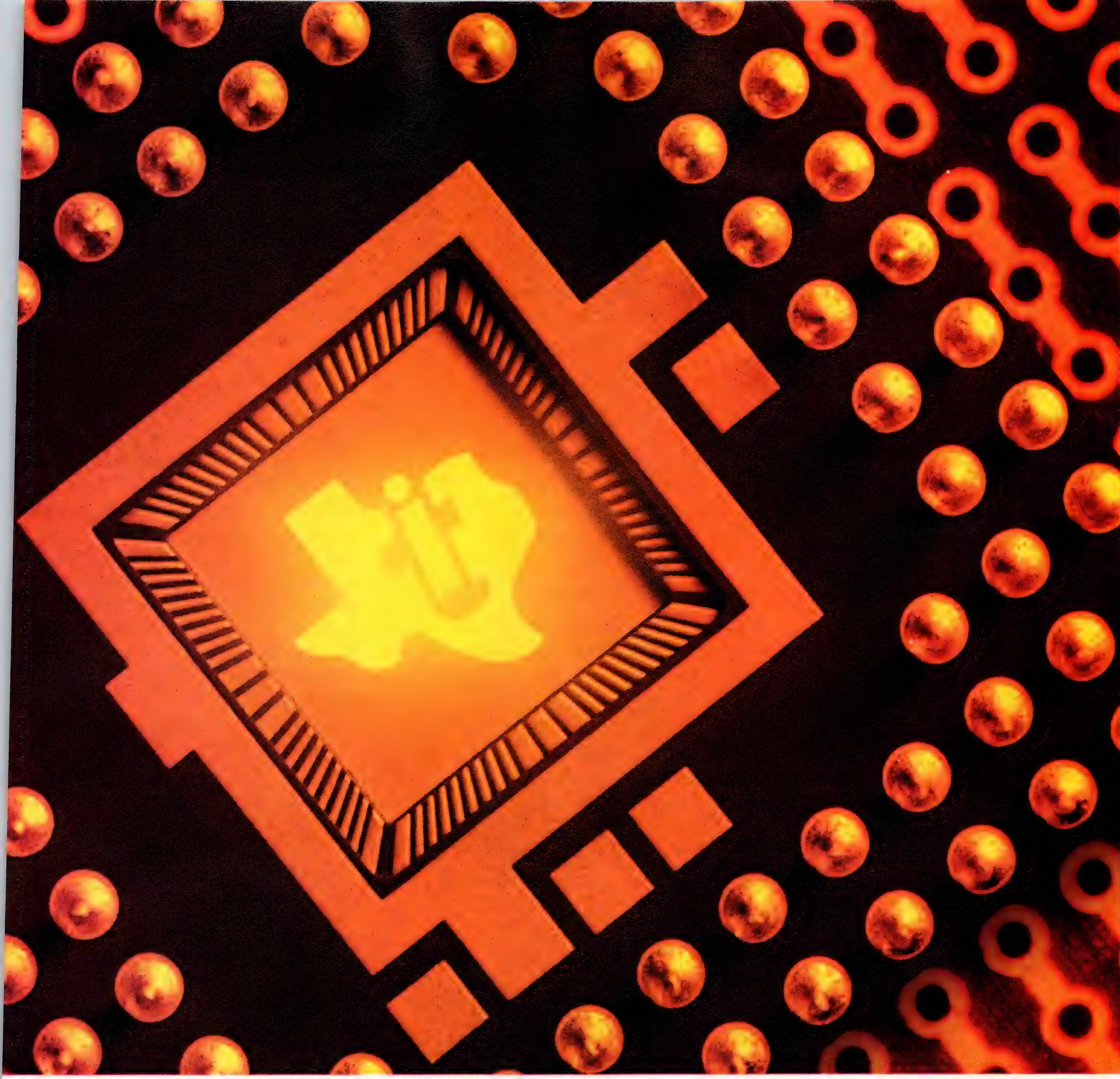

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Acknowledgment of front-cover artwork

Burtek Corp provided Telesoft with the initial artwork that Telesoft modified with Business Art for the front cover (EDN, August 17, 1989). The picture shows a flight simulator for the C-141B airplane developed by Burtek. It is programmed using a Gould Concept 32/9780 computer and Telesoft's GeleGen2 Ada Development System.

Distinguish erasing methods for flash memories

In the Special Report on Nonvolatile memories (EDN, September 1, 1989, pg 100), Michael Markowitz fails to make an important distinction between erasing methods for flash memories from different vendors. His statement "Flash memories require that as the first part of your erase algorithm, you program all the bytes to data 00_h to equalize the charge on all transistors" is too broad; it is actually true only for the Intel devices. SEEQ's and National Semiconductor's flash memories have integral select devices in each bit; this configuration eliminates the need to equalize the charge on all bits by programming before erasure. TI's part also doesn't require this extra step.

Mike Villott
Vice President and General Manager
SEEQ Technology Inc
San Jose, CA

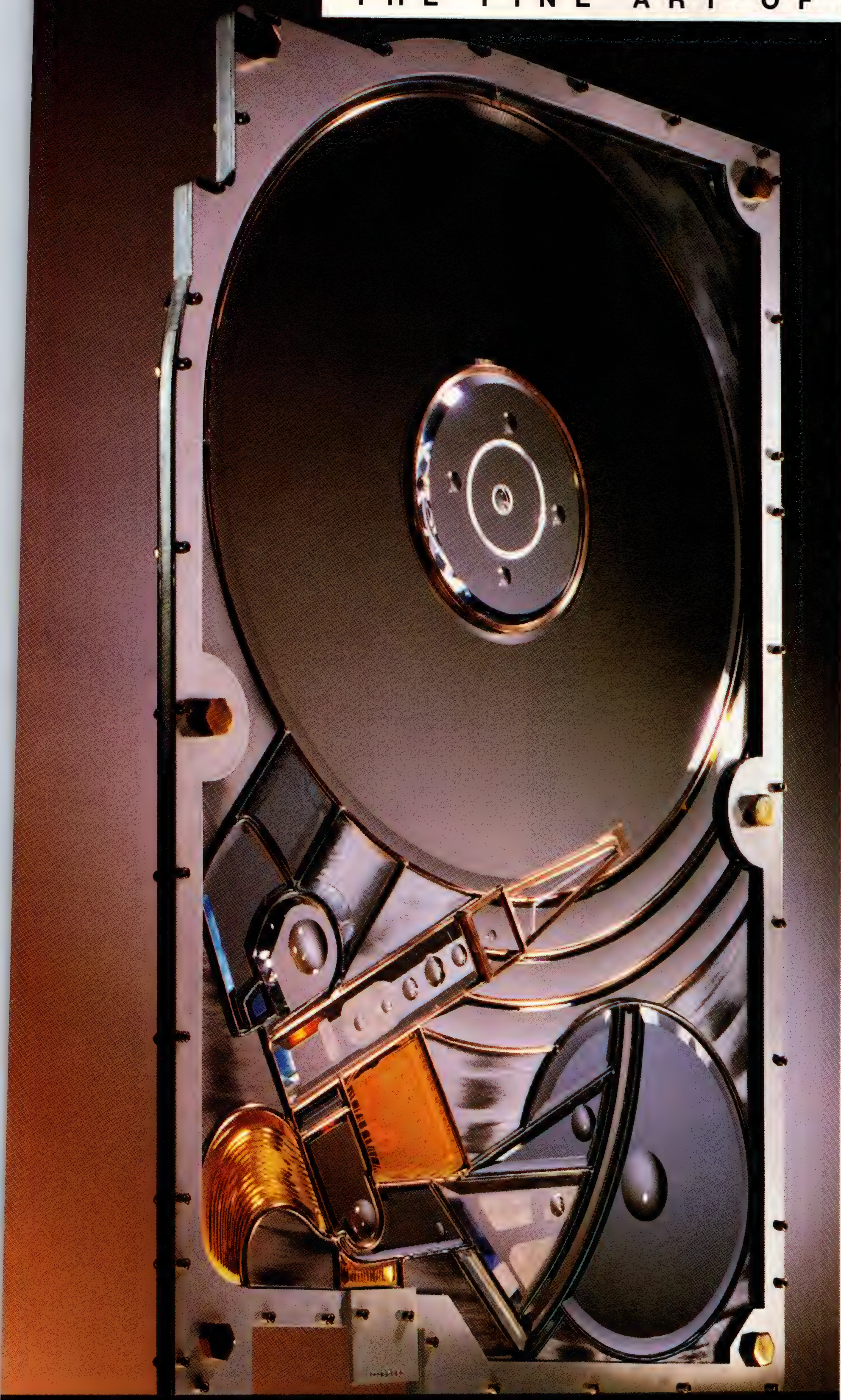
An apology for confusion over diode

In Part 6 of my series on troubleshooting analog circuits (EDN, August 3, 1989, pg 129), I'm afraid I made one verbal short cut too many. I refer to a "diode-connected transistor," then in the next line I talk about the "emitter-collector diode." In both cases, I am talking about the connection where the transistor's base is tied to the collector. The emitter is the opposing electrode. Every modern transistor connected in this fashion behaves as a very fast-switching diode, but it is one horrible beast to describe unless you spell everything out in great detail. The editors and I were hoping that the way I wrote it would be clear, but apparently I succeeded in confusing some people, and I apologize. Sometimes engineering slang really is not precise enough. (I guess if that's the worst writing I've done in all those pages, I'll take my lumps.)

Robert A Pease
Staff Scientist
National Semiconductor
Santa Clara, CA

Seagate's ST1096 Family

THE FINE ART OF DISC DRIVES



Beveled Glass Window by
Thomas Tisch & Andreas Lehmann
Oakland, California

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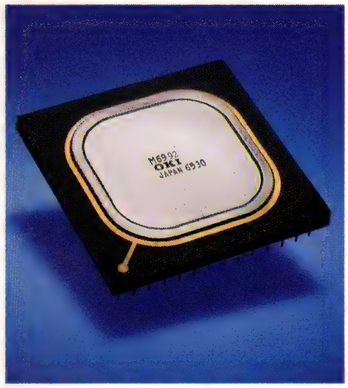
▶ *Development System*—the PSP92 permits real-time processing of analog signals through separate "digital" and "analog" PC-AT cards. It also allows for sophisticated 16-color EGA-compatible graphics.



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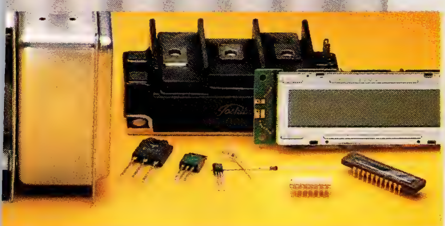

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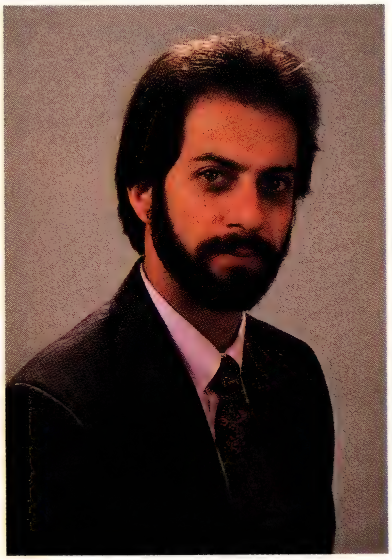

Perhaps you had a chance to read *Forbes* magazine's recent list of the top 40 entertainers. If you missed the list, here's a quick summary: In its search for the 40 most successful entertainers over the past two years, *Forbes* estimated that Michael Jackson earned a staggering $125 million. Steven Spielberg made around $105 million and Bill Cosby took in about $95 million. My income doesn't come close to any of these figures, and I'm fairly sure yours doesn't either. Though engineers, like entertainers, are valued for their creativity and productivity, we all probably earn considerably less than $100,000.

Of Bill Cosby's income, *Forbes* guessed that the talented Dr Cosby took in $4 million *per month* from syndication rights for reruns of TV's popular "The Cosby Show." According to the list's authors, Cosby can expect to receive $167 million in syndication fees by 1992.

Or consider the Rolling Stones. They ranked 8th on the list by earning about $55 million over two years—$11 million in 1988 when their current tour was just a twinkle in the eye of its promoters. In addition, and without much effort, the group collects about $1.75 in royalties for every Rolling Stones record, tape, and CD that is sold. They also earn a nickel every time one of their recorded songs is commercially played.

In my previous engineering jobs, I was on a team that designed a popular DSP chip. I also headed a group that worked on high-volume sound-generating chips and I've designed a number of ASICs. And while my previous employer has been reaping the rewards of my—and others'—intellectual performances, my share of the royalties has been one free lunch.

Do any of us know who created the compact disc, the microwave oven, or the fax machine? Who can name the engineers who designed Intel's 4004 microprocessor? It's safe to say that the nameless designers and design teams that worked on the products above have done more for the collective good of the world than Messrs Jackson, Spielberg, and Cosby. If you doubt me, imagine what the world would be like without these three individuals. Now imagine what the world would be like without microprocessors. Unfortunately, I doubt that many of the engineers involved in any 20th-century innovations have shared in the profits or rewards from their discoveries, developments, or designs. Thus, their "recorded performances" have given them a royalty of $0.

The value our society places on professional job performance and on what professionals produce is obviously out of kilter. We have to wonder about a society in which top entertainers, using their developed skills and talents, can command salaries that are so much higher than those paid to engineers. Today, almost all engineers sacrifice meaningful royalties when they go to work for an employer. We think that such a sacrifice is wrong and that it must stop. Now is the time for design engineers to start negotiating for a percentage of the earnings from their finished projects.

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VXIBUS PRODUCT ROUNDUP

182 VXIbus products appear from 36 firms

A bumper crop of products presages a smooth ride for the instrumentation bus, but don't get the idea that VXI has jumped all the hurdles yet: some nagging uncertainties still lurk ahead.

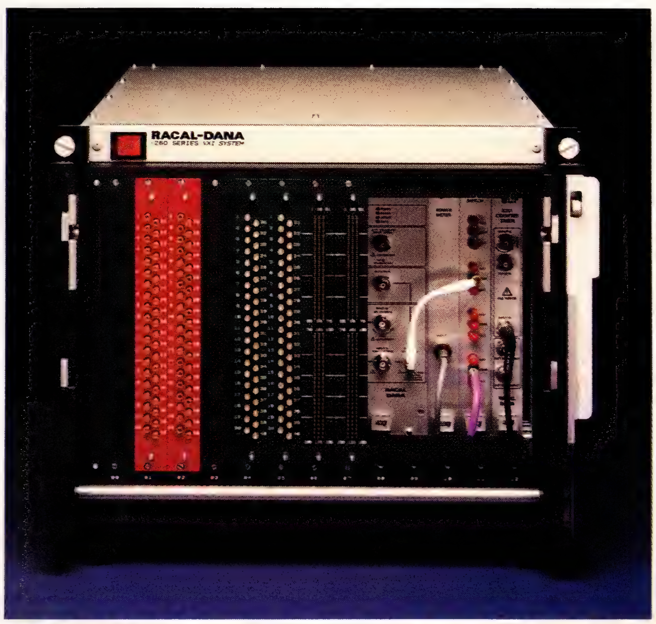
Dan Strassberg, *Associate Editor*

EDN's first roundup of VXIbus products contains 182 entries from 36 vendors. Considering the newness of the modular-instrumentation standard—the original version appeared less than 2½ years ago, with the first VXI product announcements following about six months later—the number of products is a good omen for the future of the instrumentation bus. Although VXI has many more tests to pass, the standard appears headed for success.

To compile the listing, we contacted over 140 people at companies that had requested VXI vendor identification numbers before June 30, 1989. In addition to information on products now in production, the roundup includes data on products with planned first deliveries in the first half of 1990.

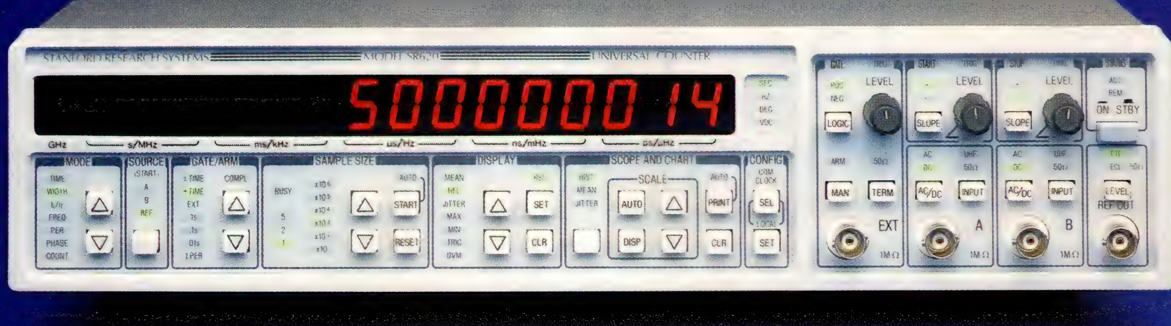
Of the 182 products listed in **Table 1** (pg 60), we classified 53 as chassis, enclosures, backplanes, prototyping aids, power supplies, and adapters. Another 28 are computers, VXI interfaces, slot-0 boards, resource managers, and peripheral controllers. Ten are systems, eight are software packages, and 83 are instruments that we classified into 13 categories. The most numerous instruments are relay switching boards (16) and digital I/O boards (13). The listing includes nine counters, eight digital multimeters and related instruments, and three high-speed waveform digitizers—the closest thing you'll find to a scope in the VXI world.

A year ago, you'd hear lots of comments about how long you'd have to wait before you could build a useful test system from VXI modules alone, and that for the foreseeable future, you would have to combine VXI modules with conventional rack-and-stack instruments. Eighty-three instruments is certainly a small number when compared with the thousands of rack-and-stack products you can buy, but only a few of the most popular instrument types are not



A C- or D-size VXI system, *like this one from Racal-Dana, has 13 slots. Modules can occupy more than one slot, however. This system contains a 2-slot-wide module (visible to the right of center).*

Time interval measurement. $3850.



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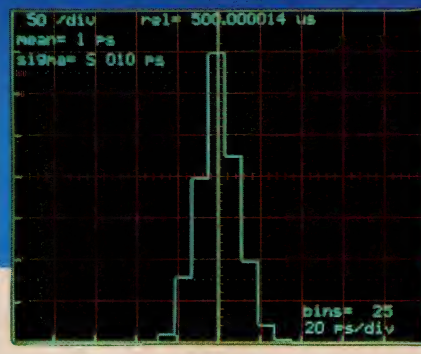

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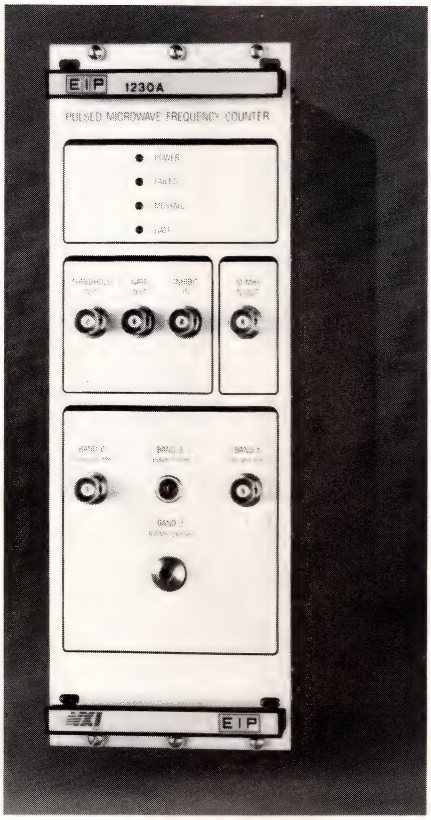


Just because an instrument is compact *and modular doesn't mean it has to offer low performance. This pulsed microwave frequency counter from EIP Microwave operates to 170 GHz.*

represented; aside from MIL-STD-1553 bus analyzers, no emulation-test tools, such as in-circuit emulators, appear in the list. Also, the roundup features no logic analyzers, spectrum or network analyzers, or ac impedance-measuring instruments.

The history of the VXIbus is something of an anomaly. In a mature market like test and measurement, you expect to find marketers setting strategy and engineers implementing it. But the VXIbus didn't begin with marketers; it began in early 1987 with a group of engineers getting together almost surreptitiously and writing a specification. They based the specification on the VMEbus and named the standard VXI (VME extensions for instrumentation). Only after the details had been hammered out were marketers invited to join the party. Normally, competing firms don't cooperate, but the engineers who drafted the VXI specification came from companies that usually compete ferociously.

The engineers who wrote the VXI specification knew they had to act fast, because they sensed that they had only a brief window of opportunity to create a modular-instrumentation standard that would be acceptable to the Air Force and usable in commercial applications.

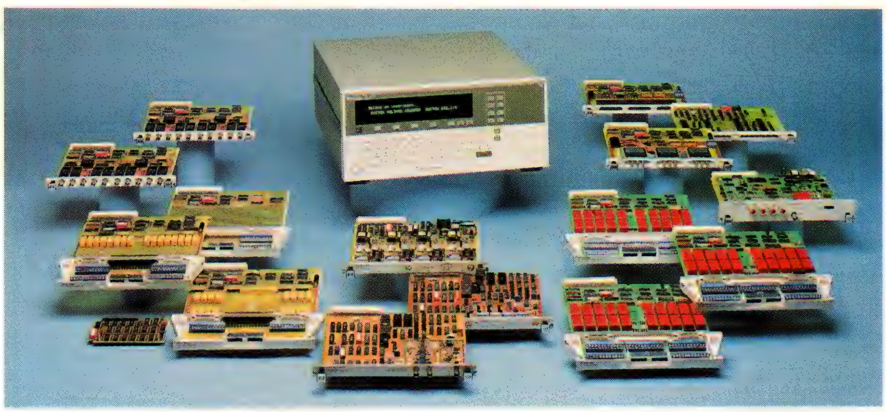
The group that originally drafted the VXI specification has evolved into the VXI Consortium, now organized as a nonprofit corporation. Voting membership (called sponsorship) is open to companies that are working actively in the field, that want to invest the $25,000 initiation fee, and are willing to devote substantial effort to the consortium's work. Nonvoting membership involves a smaller commitment of both money and time.

A firm doesn't have to be a consortium member to supply VXIbus products, however, and most of the vendors that responded to EDN's survey aren't members. The box **For more information . . .** indicates those firms that are members. It also contains the address of the consortium and that of Bode Associates, a charter member of the consortium and publisher of the VXIbus Newsletter. The newsletter, which costs $195/year, is a valuable source of information about VXI products and consortium activities.

VXIbus still faces problems

The most vocal VXI proponents would like you to believe that the bus has now jumped all the major hurdles, which simply isn't true. Though VXI has cleared some significant hurdles, it must overcome many more. No vendor has yet recouped its investment in developing VXI products, and the chances are slim that in 1990 any vendor's profits from VXI will exceed the development costs it has incurred. Indeed, the prospect of elusive profits is probably the reason why several of the founding members of the VXI consortium have yet to announce their first VXI products.

One area that many potential users feel the VXI standard failed to address adequately was how to build reasonably large systems. A full-rack-width, C- or D-size VXI card cage (mainframe) holds, at most, 13 modules (cards), of which



VXI products needn't be expensive *as these B-size units from Hewlett-Packard demonstrate.*

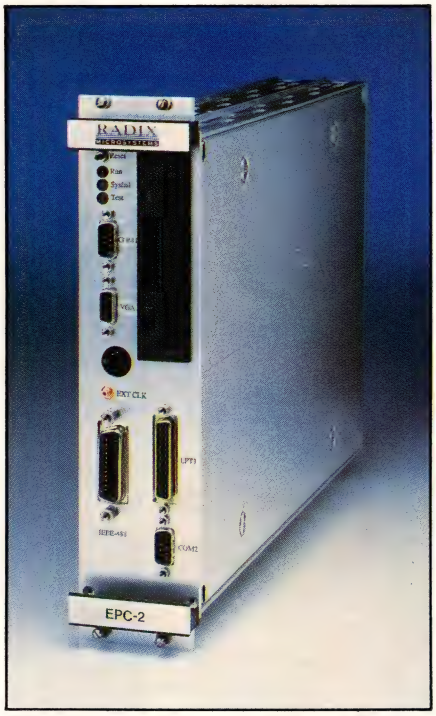
one is a resource manager. The standard defines four card sizes, with the largest—the D size—measuring 13.38 by 14.43 in. However, no provision exists, even in the latest revision (version 1.3), for synchronizing more instrumentation cards than will fit in one mainframe.

MXI syncs multiple mainframes

National Instruments has addressed this problem by proposing the MXI bus, an extension to VXI that allows synchronization of cards in multiple mainframes and communication with an external computer at speeds higher than those achievable via an IEEE-488 interface. The firm is offering MXI as an open standard and hopes that the VXI consortium will adopt it.

Another problem with the bus was that most of the products offered for it, until this summer, were so expensive that they were likely to find applications only in military test equipment. The announcements of these products conveyed the impression that you had to pay rather dearly for *giving up* a front panel you could use when all else failed. Most early VXI products cost more than their rack-and-stack counterparts. Yet the VXI versions, which lack not only front-panel controls but also a case and power supply, require that you create or obtain controlling software and purchase a VXI mainframe, a computer, and a resource-manager board.

Recently, however, a number of lower-cost VXIbus modules have emerged, including more than a dozen in the form of B-size cards from Hewlett-Packard. Most of these cards are register based as opposed to message based. Many offer fewer functions and looser specifications than their C-size



***The computers that control VXI systems** can be external or internal. This VXI module, from Radix Microsystems, is a complete 80386-based PC with a floppy-disk drive, a 40M-byte hard drive, and a VGA display adapter. It also functions as a VXI resource manager.*

counterparts. Whether such medium-performance units will gain wide acceptance remains to be seen. According to Don Chase, the product marketing manager for the Data Acquisition Group at Analogic Corp, several VXI vendors have told him categorically that register-based architectures will never succeed in the VXI world. Chase claims that companies that hold this viewpoint haven't taken the trouble to appreciate the power of the register-based architecture allowed under VXI, and its potential to enable the creation of fast, powerful, easy-to-use modules.

The topic of register-based vs message-based architectures leads to the subject of instrument-control software. The VXIbus, with its open hardware architecture, its emphasis on the interoperability of modules from different vendors, and its *requirement* that you use software to control module operation, really forces the most significant issues in instrumentation out of the arena of hardware and into that of software. Unless the vendors of instrument-control software develop a strategy for providing drivers for the hundreds of VXI modules that will surely exist in the next few years, many users will find the concept of an open-architecture system to be a tantalizing mirage rather than a reality.

If you object to creating software drivers for new instruments, you must make sure that you'll be able to obtain drivers for all of the hardware modules you can reasonably expect to use over the life of your system. You have to evaluate a potential software vendor's commitment to support many manufacturers' hardware, or the commitment of potential hardware suppliers to support your chosen software. An instrument-control package that supports only one vendor's hardware can lock you into a single hardware source, even though you thought that by selecting VXI you had committed to an open hardware architecture.

Recently, HP made an announcement calculated to ease the software problems associated with incorporating multiple vendors' hardware into VXI systems. HP announced that for a nominal fee it would license other vendors to use—and extend without HP's prior approval—an instrument-command syntax called TMSL (test-and-measurement systems language).

TMSL's goals are ambitious. HP is attempting a feat at which nobody else has ever really succeeded: the creation of a truly universal, instrument-command syntax. If TMSL

works as HP hopes, you'll be able to upgrade the instruments in your system without modifying the instrument-control programs you've written. For example, the commands to make a frequency measurement with a counter and a spectrum analyzer are the same, so if today you use a counter to measure frequency, and next year you remove the counter from your system and install a spectrum analyzer, the system will continue to run correctly under the control of your original program.

Questions remain about whether other vendors will extend the syntax without corrupting it, and potential users have asked whether the universal command set will impose speed penalties on instrument operation. Answers to some of these questions should soon start to emerge: HP has stated that all of its VXI instruments (and all of the rack-and-stack instruments it develops from now on) will support TMSL.

A new storm is brewing over microwave instruments for use in VXIbus-based systems. About a year ago, HP opened the architecture of its 70000-series modular microwave measurement system (MMMS) and offered the packaging and interfacing scheme as an adjunct to VXI. HP claims that VXI isn't well suited to microwave instruments. Since HP was one of the firms involved in drafting the VXI standard and is one of the standard's strongest proponents, you can't easily ignore the company's claims.

Opening the 70000 architecture consisted of making internal documentation available for a nominal charge, selling mechanical parts to companies that want to use them to build prototypes, and permitting the company that fabricates the

For more information . . .

For more information on the VXIbus products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following vendors directly, please let them know you saw their products in EDN.

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HP-designed interface ICs used in the system to sell them on the open market.

Partly as a result of this move, HP landed a substantial military subcontract (with General Electric), and a handful of other vendors have gone on record as supporting the 70000 architecture as the preferred means of incorporating microwave instruments in VXIbus-based systems. Other firms, such as Tektronix, have stated that there is no need to use a separate packaging scheme to accommodate microwave instruments in VXI systems; also, they believe that adoption of the 70000 architecture as an adjunct to the VXIbus would give HP an unfair advantage.

These vignettes emphasize the unusual nature of the VXI community: Many VXI vendors are longtime rivals, but despite their occasional differences, they share a unique sense of purpose where VXI is concerned. Because they want—and expect—VXI to succeed, they're willing to go the extra mile to help users. Also, many of the people you'll deal with at VXI suppliers are engineers themselves. They know that it was a group of working engineers—not marketers or accountants, and not an IEEE standards committee—that found an innovative way for competitors to cooperate. Vendor personnel who support VXI feel that, because of VXI's origins, the success of the bus will be a triumph for engineers.

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Tables begin on pg 60.

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FAX (972)3-492190
Circle No. 440

Radix Microsystems Inc
1945 NW Von Neumann Dr
Beaverton, OR 97005
(800) 950-0044; in OR, (503) 690-1229
FAX 503-690-1228
Circle No. 441

Schroff Inc
170 Commerce Dr
Warwick, RI 02886
(800) 451-8755; in RI, (401) 732-3770
FAX 401-738-7988
Circle No. 442

Standard Logic Inc
4940-A E LaPalma Ave
Anaheim, CA 92807
(714) 779-2897
FAX 714-779-3499
Circle No. 443

Struck Electronics
Box 12 61
D-2000 Tangstedt, West Germany
4109 5517
FAX 4109 5533
Circle No. 444

Tasco Electronic Services Inc
2121 W Crescent Ave
Anaheim, CA 92801
(714) 635-0550
FAX 714-535-3458
Circle No. 445

Tektronix Inc*
Box 3500
Vancouver, WA 98668
(800) 433-2465
FAX 206-253-6075
Circle No. 446

Tracewell Enclosures Inc
567 Enterprise Dr
Columbus, OH 43081
(800) 848-4525; in OH, (614) 846-6175
Circle No. 447

Transmagnetics Inc
210 Adams Blvd
Farmingdale, NY 11735
(516) 293-3100
FAX 516-293-3793
Circle No. 448

Unipower Corp
2981 Gateway Dr
Pompano Beach, FL 33069
(305) 974-2442
FAX 305-971-1837
Circle No. 449

Universal Test Equipment
1242 W Lincoln Ave, Unit 8
Anaheim, CA 92805
(714) 956-5337
FAX 714-956-7250
Circle No. 450

VME Development Corp
1842 W Grant Rd, Suite 108
Tucson, AZ 85745
(602) 624-8012
FAX 602-624-2880
Circle No. 451

VXIbus Consortium Inc
Box 1736
Vancouver, WA 98668
FAX 206-253-6075
Circle No. 452

Wavetek Corp*
9145 Balboa Ave
San Diego, CA 92138
(619) 450-9971
FAX 619-450-0325
Circle No. 453

Westcor Corp
485-100 Alberto Way
Los Gatos, CA 95032
(408) 395-7050
FAX 408-395-1518
Circle No. 454

*Corporate members of the VXI Consortium. (Several consortium members, including some founding members, don't appear because they don't yet offer VXIbus products.)

Table 1—VXIbus Products

Use Table 1 as the first step in locating the VXI products appropriate for your application. The table contains a condensed statement of each product's most significant attribute. Abbreviations in the table that aren't commonly used in EDN are decoded in the notes after the table.

When using the table, remember that the classification of products by type is somewhat arbitrary. A microwave counter is listed as a counter, but it could just as well have been called an RF and microwave instrument. When trying to locate a particular type of product, look under all of the classifications that might contain it.

Vendor	Model	Size[2]	Major characteristic(s)	Base US list price[3]	First shipment
			ADCs, fast digitizers, related units		
Analogic	DVX2502	B1	8-channel, 16-bit, 200k-sample/sec ADC	$3700	6/89
	DVX2601	B1	16 16-bit, differential-input S/H circuits	$3600	10/89
Tektronix	VXI5260	C2	2-channel, 200M-sample/sec, 8-bit ADC	$10,950	9/88
			Chassis, enclosures, backplanes		
Bicc-Vero	203302533		13-slot, powered, cased, C-size cage	$6586	4/89
	203303169		13-slot, powered, uncased, C-size cage	$6347	9/89
	63302183H		6-slot, 10-layer, C-size backplane	$764	2/89
	63302182L		13-slot, 10-layer, C-size backplane	$1296	11/88
	63302880D		13-slot, 10-layer, D-size backplane	$2167	9/89
Colorado Data Systems	73A-021		Powered C-size cage	$5995	1/88
Hewlett-Packard	E1300A		Powered mainframe; 7B, 3A slots	$2300	11/89
	E1301A		Like E1300A but has controls, display	$2800	11/89
	E1400B		Powered C-size mainframe, 13 slots	$6275	1/90
Interlogic Industries	VXIJ1J2-5		5- and 13-slot backplanes with ECL clock buffer and active summing-bus protection	$596	8/89
	VXIJ1J213			$1037	8/89
National Instruments	VXI-1000		5-slot, C-size, powered VXI mainframe	$3600	9/89
Racal-Dana Instruments	1261		C-size VXIbus chassis	$6450	1/89
	1262		1261 with I/F for 12 connector blocks	$9875	1/89
Schroff	8U Rack		13 C-size slots; 24-in. deep	$3995	6/89
	20800-250		10-slot C-size backplane. Meets VXI 1.3	$1150	4/89
	20800-253		13-slot C-size backplane. Meets VXI 1.3	$1310	4/89
Standard Logic	110701		Subracks w/o backplane; all sizes	$108	
	110861-3		7-layer backplane	$992	1988
Struck	STR8001		Powered C-, D-size 7-slot card cages	$6000[4]	10/89
	STR8002		Powered C-, D-size 13-slot card cages	$7500[4]	12/89
Tektronix	VXI1405		5-slot, powered, C-size mainframe	$3600	Q2/89
	VXI1500		13-slot, powered, D-size mainframe	$9995	8/89
Tracewell Enclosures	23/I		Powered C-, D-size 13-slot mainframes.	$6900	8/89
	23/II		Power to 1500W. Backplanes have 14 layers	$8900	8/89
Universal Test Equipment	VX-000		Powered A-size chassis with controller	$2995	12/89
			Computers, slot-0 boards, peripherals		
Colorado Data Systems	73A-151	C1	Slot-0 card with IEEE-488 interface	$2495	1/88
	73A-156	C1	Slot-0 card that acts as MATE ICM	$2595	3/89
	73A-160	C4	12-MHz '286 CPU, slot-0, IEEE-488 interface	$4995	5/89
	73A-152	C1	'186-based CPU for user's software	$3295	
	73A-931		640×200-pixel EL display (see text)	$1995	5/89
	73A-932		101-key "enhanced" keyboard	$140	5/89

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D/R	digital-to-resolver
form-C	spdt break-before-make
I	current
IAC	instrument on a card
ICM	Instrument Control Module
MATE	Modular Automatic Test Equipment
opt	optional
ppb	parts per billion
R	resistance
R/D	resolver-to-digital
S/R	synchro/resolver
w/o	without
Z	impedance

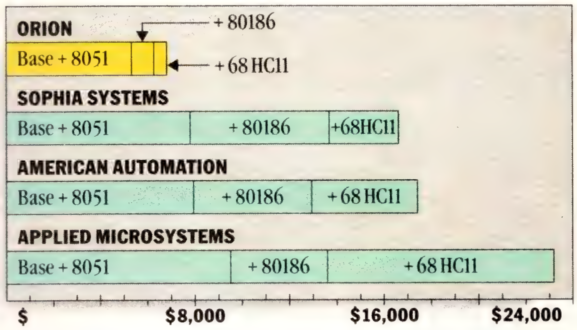
Table continued

How To Get More Emulation For Less

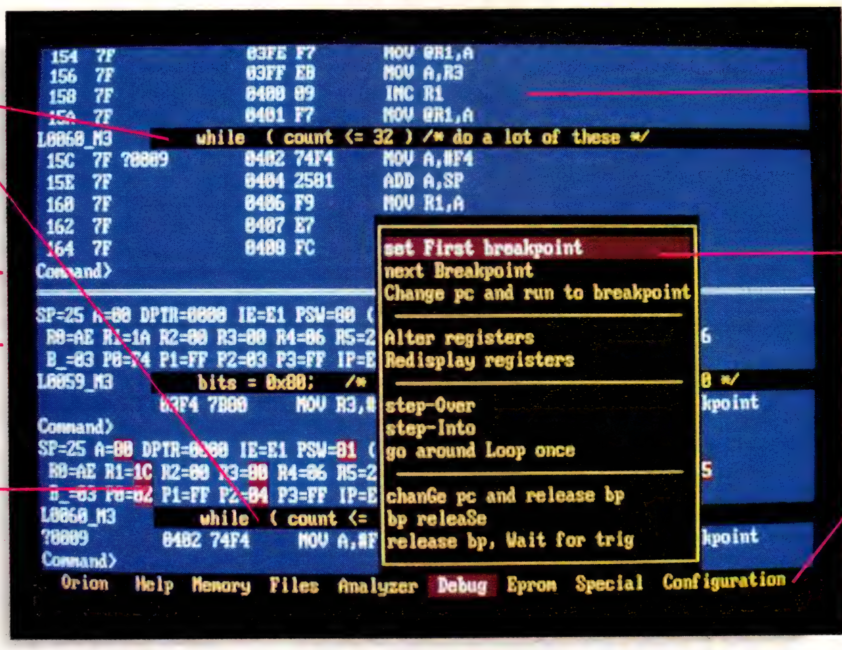
More Emulation

	ORION	OTHERS
Sophisticated Trace Triggering/Debug by Symptom	Standard	Optional
Hi-Level Language Symbolic Debugging	Standard	Optional
Real Time Processor Function Monitoring	Yes	No
Extensive Macro Capabilities	Yes	No
Support For Over 170 Microprocessors	Yes	No

Less Cost



ORION 8620



HIGH-LEVEL language source lines and symbols are shown in both the disassembled trace and break-points.

SPLIT-SCREEN display provides multiple work areas and different views of data.

BREAKPOINT shows register contents and allows modification; registers are highlighted as they change.

ANALYZER TRACE triggering shows realtime instruction execution enabling you to debug by symptom.

DEBUG POPUP gives immediate access to break-points, single-steps and all debug functions.

POPUP MENUS make the 8620 the easiest development system to learn and use.

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ORION INSTRUMENTS

Table 1—VXIbus Products (Continued)

Vendor	Model	Size[2]	Major characteristic(s)	Base US list price[3]	First shipment
			Computers, slot-0 boards, peripherals (continued)		
Evira	EVLAN-21	B1	Ethernet controller for OS/9 or TCP/IP	$1495	9/89
Hewlett-Packard	E1405A	C1	Slot-0 resource manager	$2800	1/90
	E1480A	C4	68030-based CPU and resource manager		
	E1404A	C1	Slot-0 card, VMEbus system control	$850	9/88
ICS	VXI5523	C1	VXI interface 2/3 of module for user card	$700	10/89
	VXI5533	C1	Parallel VXI interface via two D connectors	$800	
National Instruments	VXI-MXI	C1	Slot-0 card. Creates MXI bus (see text)	$1995	10/89
	GPIB-VXI	C1	Allows control of VXIbus via IEEE-488	$3000	8/89
NH Research	81120	C1	Slot-0 card. RS-232C, 2 IEEE-488 ports	$5000[4]	12/89
Racal-Dana	1260-0	C1	Slot-0 resource manager	$2700	1/89
	1265	C2	'386-based CPU, VGA, RS-232C, IEEE-488	$10,000	1/90
Radix Microsystems	EPC2000	C2	'386 PC, 40M-byte hard disk, 5 ports	$9550	1/89
Struck	STR8031	C,D1	Nubus (Mac II) to VXI interface, resource manager	$8000[4]	3/90
	STR8060	C,D1	VXI interface. Can hold flash ADC, clock, RAM	$2500[4]	11/89
Tektronix	VXI4530	C2	16-MHz '386-based CPU/slot-0 card	$11,750	8/89
	VXI4535	C2	20-MHz '386-based CPU/slot-0 card	$17,500	8/89
Giordano Associates	A1028	B1	96 I/O lines each with 32k bits of RAM	$14,500	6/88
Hewlett-Packard	E1330A	B1	Four 8-bit bidirectional ports	$600	11/89
	E1364A	B1	16 form-C switches	$650	11/89
NH Research	81302	C1	16 inputs, 16 drivers, 16 dpdt relays	$4500[4]	12/89
Tektronix	VXI4440	C1	6 ports drive external RF relays	$3250	8/89
Universal Test Equipment	VX-86	A1	8 programmable unit-under-test stimuli	$595	12/89
	VX-83	A1	24-line variable-threshold logic input	$595	12/89
			Frequency sources, synthesizers		
Pentek	1620	B1	DC-to-20-MHz ±3 ppm; resolves 32 bits	$6000[5]	
Racal-Dana	1260-04E	C2	1-, 5-, 10-MHz reference, 0.5 ppb/day	$2485	1/90
	1260-04R	C2	Rubidium frequency standard	$10,950	1/90
			Frequency-domain measurements		
NH Research	81401	C1	Measures p-p ac V in 7 frequency bands	$3750[4]	12/89
	VXI5520	D1	Slot-0 card. RS-232C, 2 IEEE-488 ports	$3995	8/89
	VXI5530	D2	16-MHz '386-based CPU/slot-0 card	$17,900	8/89
	VXI5535	D2	20-MHz '386-based CPU/slot-0 card	$23,900	8/89
Universal Test Equipment	VX-57	A4	Alphanumeric display 1.2-in. characters	$595	12/89
	VX-53	A1	Controls VMEbus from RS-232C or RS-422	$595	12/89
	VX-54	A1	Like VX-53 but uses Centronix port	$595	12/89
			Digital I/O, pin drivers/receivers		
Colorado Data Systems	73A-353	C1	32 spst relays for 1 kVA ac; 90W dc	$1495	10/88
	73A-355	C1	24 independent spdt or dpst relays	$1995	11/89
	73A-356	C1	20 independent dpdt relays	$1995	10/89
	73A-357	C1	32 spdt relays otherwise like 73A-353	$1495	5/89
	73A-411	C1	48 optoisolated TTL/CMOS I/O lines	$2195	4/89
	73A-412	C1	80 nonisolated TTL/CMOS I/O lines	$1995	8/89
	73A-541	C1	10-MHz counter with time-tag memory	$2295	5/89
	73A-993	C1	160-MHz universal counter; 1.3-GHz opt	$3500	4/89

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I	current
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R	resistance
R/D	resolver-to-digital
S/R	synchro/resolver
w/o	without
Z	impedance

Table continued

Table 1—VXIbus Products (Continued)

Vendor	Model	Size[2]	Major characteristic(s)	Base US list price[3]	First shipment
Digital I/O, pin drivers/receivers (continued)					
EIP Microwave	EIP 1230A	C3	Pulsed microwave counter 100 Hz to 170 GHz	$17,400	1/90
	EIP 1231A	C3	Pulsed microwave counter 100 Hz to 20 GHz	$14,700	1/90
Hewlett-Packard	E1332A	B1	4-channel, 4-MHz counter/totalizer	$900	11/89
	E1333A	B1	3-channel, 1-GHz counter	$900	11/89
Racal-Dana	2151	C2	9-digit, 20-GHz microwave counter	$4585	1/89
	2251	C1	9-digit, 1.3-GHz universal counter	$3250	1/89
Tektronix	VXI4223	C1	160-MHz universal counter; 1.3-GHz opt	$3500	8/89
MIL-STD-1553 products					
Colorado Data Systems	73A-453	C1	MIL-STD-1553 simulator/tester	$3400	9/88
Digital Technology	DTI-2180	C1	MIL-STD-1553 interface, terminal emulator	$9500	3/90
ILC Data Device	BUS-65522	B1	1553 Bus controller/terminal/monitor	$4995	9/88
Power sources, loads, resistors					
Colorado Data Systems	73A-342	C1	Programmable R: 10Ω to 500 kΩ	$1895	9/88
NH Research	81201	C1	Load: 50W, 1A	$2500[4]	12/89
	81210	C1	Load: 50W, 10A	$2500[4]	12/89
Struck	STR8042	D1	Message-based R decade: 0-150Ω/15 kΩ/1.5 MΩ	$4500[4]	8/89
Universal Test Equipment	VX-149	A1	Programmable R—1Ω (10W) to 6 MΩ	$595	12/89
Power supplies for VXI mainframes					
Unipower	PH Series		Output to 1 kW: 5, ±12, ±24, −5.2, −2V	$655	5/89
Westcor	SP7-1801		3.2×5.5×11.5-in., 8-output 1200W supply	$1950	2/89
Prototyping hardware, adapters					
Bicc-Vero	63302203B	C1	C-size, wrappable, prototype board	$1077	4/89
	63303103A	C1	Wrappable prototype board with VME interface		9/89
	206303183	C1	Allows mounting B card in C backplane		9/89
	63302270E	B,C1	4-layer module-extender board	$746	4/89
Colorado Data Systems	73A-451	C1	Prototyping module with interface	$895	5/88
	73A-452	C1	Prototyping module without interface	$495	6/88
	73A-851	C1	VME to VXI with address, data buffers	$995	9/89
	73A-852	C1	VXI adapter for vendor's 53/63 series	$495	1/88
Hewlett-Packard	E1399A	B1	Breadboard with register-based interface	$400	11/89
	E1490A	C1	Same function as E1399A—larger size	$500	9/88
	E1408A	C1	Mounts A or B module in C-size slot	$170	9/88
	E1402A	C1	Mounts VME B-size card in VXI C slot	$550	1/90
	E1409A	C	C-size intermodule shield	$150	9/88
ICS	VXI-5500	C1	Prototype module with separate interface board	$750	12/89
Interlogic Industries	EXT6U-340		B-size passive extender	$350	8/89
	EXT9U-340		C-size passive extender	$390	8/89
Radix Microsystems	EPC-2AM	C1	Lets you plug IBM PC bus cards into VXI	$400	6/89
Standard Logic	31C4-64D4	ABCD	4-layer boards for wrapping, stitching	$271	1988
Struck	STR8011	C,D1	Wrappable 2-layer prototype boards	$600[4]	8/89
	STR8023	C,D1	Passive bus extender; front test points	2500[4]	9/89

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w/o	without
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Table continued

Table 1—VXIbus Products (Continued)

Vendor	Model	Size[2]	Major characteristic(s)	Base US list price[3]	First shipment
			Prototyping hardware, adapters (continued)		
Tektronix	VXI1321	B1	Development module with bus interface	$1950	
	VXI1421	C1	Development module with bus interface	$2150	
	VXI1510	D3	Converts 3 VXI D slots to 4 VME B slots	$2995	8/89
	VXI1520	D2	Solderable prototype board; no bus interface	$1395	8/89
	VXI1521	D1	Development module with bus interface	$2250	
			RF and microwave instruments		
California Avionics	9900	C2	DC-to-500-MHz amplifiers, attenuators	$2700[4]	6/90
Hewlett-Packard	E1416A	C1	100-kHz to 50-GHz power meter		
	E1368A	B1	Three 18-GHz, spdt, 50Ω switches	$2100	11/89
	E1369A	B1	Drives 1368A or external switches	$500	11/89
Quartzlock Instruments	dB125-VXI	6	125-dB, 1-GHz attenuator	$3500[5]	5/89
			Signal sources, DACs		
Colorado Data Systems	73A-256	C1	12-channel, 16-bit DAC	$3295	10/88
	73A-270	C1	2-channel pulse-pattern generator	$3295	6/89
Giordano Associates	A1002	B1	4 15/25-MHz A/D stimulus/response lines	$15,000	1/88
Hewlett-Packard	E1328A	B1	4 isolated, 16-bit V- or I-output DACs	$1100	11/89
	E1440A	C2	Synthesizes functions, sweeps at 21 MHz		
Quartzlock Instruments	181-VXI	6	20-MHz synthesized-function generator	$5000[5]	
Tasco	TVXI/STM5	6	Serial word generator, analyzer	$15,000	6/89
Tektronix	VXI5790	D1	100-MHz, 10-bit waveform generator	$7995	8/89
			Software		
Hewlett-Packard	E2000A		Test generator for MS-DOS and HP 9000	$995	10/88
	E2001A		Instrument drivers for E2000A		
National Instruments	LabWindow		Instrument control in QuickBasic, C	$495	10/89
	LabVIEW		Macintosh icon-based instrument control	$1995	8/89
NH Research	Powerflex		For power-supply test. IBM PC-based		12/89
Radat Systems	Artest		For programming, debugging of ATE	$1500	6/88
Tektronix	TekTMS		PC-based test-management system	$2995	10/89
Universal Test Equipment	VXS-1		PC-based. Controls VX-000, 8 cards	$1595	12/89
			Specialized and miscellaneous products		
Tasco	TVXI-429	C	16 ARINC-429 communications channels	$7500	3/90
			Switching matrices, multiplexers		
Analogic	DVX2701	B1	Multiplexer: 32 differential channels	$995	10/89
C&H	HF4X8	B1	4-line-by-8, expandable, 100-MHz multiplexer	$1095	Q1/90
Colorado Data Systems	73A-332	C1	36-channel, 2-wire scanner	$1995	12/89
	73A-372	C1	11 units can slave to 73A-332	$1495	12/89
Hewlett-Packard	E1345A	B1	16-channel relay multiplexer	$650	11/89
	E1347A	B1	Thermocouple relay multiplexer	$750	11/89
	E1460A	C1	64-channel, 4-wire relay multiplexer	$2400	1/90
	E1346A	B1	48-channel, single-ended relay multiplexer	$800	11/89
	E1366A	B1	Two 1×4, 1.3-GHz, 50Ω multiplexers	$850	11/89

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w/o	without
Z	impedance

Table continued

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Table 1—VXIbus Products (Continued)

Vendor	Model	Size[2]	Major characteristic(s)	Base US list price[3]	First shipment
Switching matrices, multiplexers (continued)					
Hewlett-Packard (Cont.)	E1367A	B1	Two 1×4, 75Ω, 1.3-GHz multiplexers	$850	11/89
	E1472A	C1	Six 1×4, 3-GHz multiplexers	$2500	1/90
	E1473A	C1	Six 1×4 multiplexers; expands E1472A	$1500	1/90
	E1361A	B1	10-MHz, 4×4 relay matrix	$650	11/89
Matrix Systems	10081	C1	625-MHz, 4×8, coaxial matrix	$3000	Q4/89
NH Research	81301	C1	16 isolated inputs; 3 outputs; 100 MHz	$2500[4]	12/89
Racal-Dana	1260	C1	Family of relay signal-switching cards	$1395	1/89
Synchro/resolver/phase instrumentation					
ILC Data Device	IAC-37001	C1	Synchro simulator and indicator	$6995	Q1/90
North-Atlantic Industries	5388	C1	Indicates angle; simulates synchro	$5500	11/89
Transmagnetics	5410C30	C1	0.001° angle meter, 2 synchro simulators	$6500	7
	5410C-31	C1	Wideband phase-angle voltmeter	$9500	7
	5410-C42	C1	8 D/R and 1 R/D converters (12 bits)	$7500	7
	5410C-43	C1	6 R/D and 1 D/R converters (12 bits)	$6850	7
	5410C-39	C1	0.01° angle meter, S/R stimulus	$4800	7
	5410C39-1	C1	0.001° angle meter, S/R stimulus	$5500	7
Systems and multiple-module subsystems					
Colorado Data Systems	73A-ATX		Powered cage and 12-MHz, '286-based PC	$12,995	7/89
	73A-PCX		Powered C-size cage with IEEE-488 interface	$8395	
	73A-PRT		73A-PCX plus wrappable prototype board	$9995	6/88
	73A-IBX		73A-PCX less PC Bus IEEE-488 interface	$7995	6/88
	73A-MCX		73A-IBX with MATE IAC compatibility	$8995	8/89
	73S-456	C3-9	MATE-STD tester for MIL-STD-1553 bus	$8995	
Kikusui International	Final Analysis		'386-based design-verification system	$32,000	9/89
National Instruments	VXIAT2000	C1	Slot-0 card, PC/AT-MXI interface, LabWindows	$3800	10/89
NH Research	81001		IBM PC/VXIbus-based power-supply tester	$50,000	2/90
Parametric Technology	PTS4		Hybrid tester. Forces V, I; measures R, Z	$45,000	Q4/89
Voltmeters, ohmmeters, multimeters					
Hewlett-Packard	E1326A	B2	5.5-digit integrating, 14-bit fast ADCs	$1200	11/89
	E1411A	C1	Same as E1326A	$1600	1/90
	E1410A	C1	6½-digit message-based DMM	$3500	1/90
Tektronix	VXI4236	C1	6½-digit DMM from 100 nV dc, 1 mV ac	$3750	8/89
Universal Test Equipment	VX-153	A1	DMM—dc/ac V, I; ohms	$595	12/89
	VX-165	A1	Milli/micro-ohmmeter, finds short circuits	$595	12/89
Wavetek	1362	C1	6½-digit DMM, 1000 readings/sec	$3695	9/89
	1362 MT	C1	MATE-compatible version of 1362	$3995	9/89

Notes:
1. Abbreviations not commonly used in EDN appear in the list below.
2. Board format (A, B, C, or D) and number of slots occupied. If no size is indicated, the product isn't a VXI module.
3. Prices are for one piece. Where vendor indicated a price range, only the low price appears.
4. "Budgetary" (estimated) price.
5. Price won't exceed amount indicated.
6. Vendor didn't indicate size.
7. Product is in production. Vendor didn't indicate date of first shipment.

Abbreviations:
- ARINC Aeronautical Research Inc
- D/R digital-to-resolver
- form-C spdt break-before-make
- I current
- IAC instrument on a card
- ICM Instrument Control Module
- MATE Modular Automatic Test Equipment
- opt optional
- ppb parts per billion
- R resistance
- R/D resolver-to-digital
- S/R synchro/resolver
- w/o without
- Z impedance

SURFACE MOUNT MIXERS

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IF	DC-500	5-500
CONVERSION LOSS (dB)		
Midband	6.3 dB	6.5 dB
Total Range	7.5 dB	8.0 dB
ISOLATION (dB)	(L-R)(L-I)	(L-R)(L-I)
Low-Band	60 45	45 35
Mid-Band	45 40	35 30
High-Band	40 35	25 20
PRICE	$3.30 (1000 qty) $4.25 (1-9)	$4.15 (1000 qty) $5.45 (1-9)

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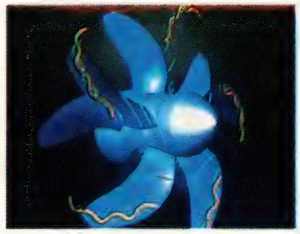
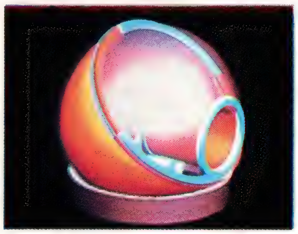


Computational fluid dynamics

Video animation productio

Video animation



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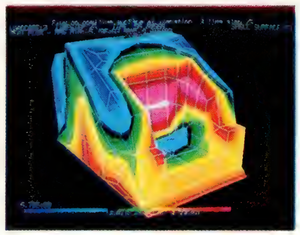
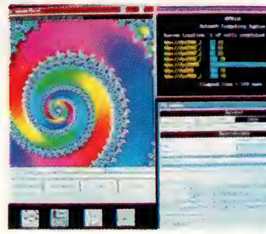


Finite element modeling and analysis



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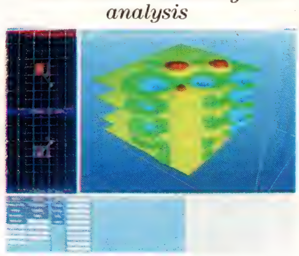
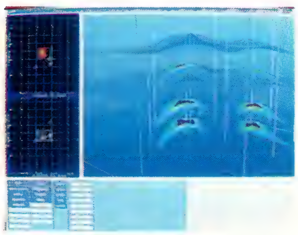
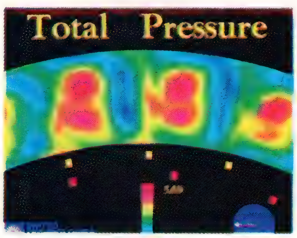


Seismic analysis

Computer-aided design in manufacturing



Reservoir analysis



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Industrial design

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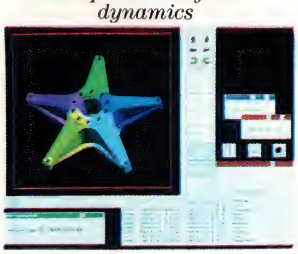

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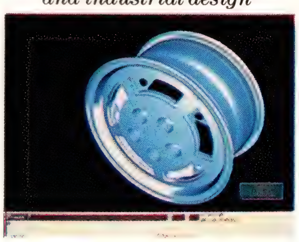
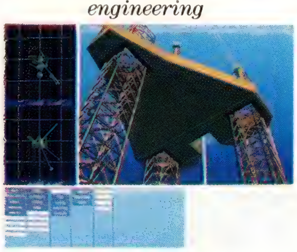
Automotive industrial design

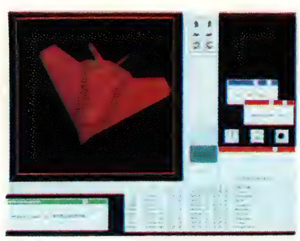
Animation



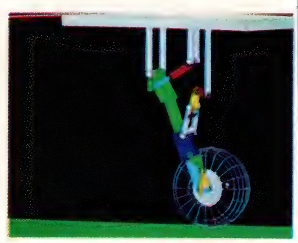
Mechanical design



Scientific visualization



Aerospace engineering



Kinematics and dynamics

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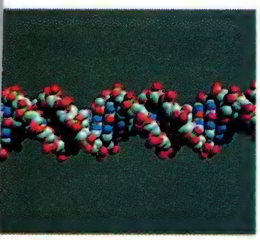

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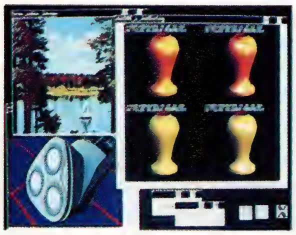
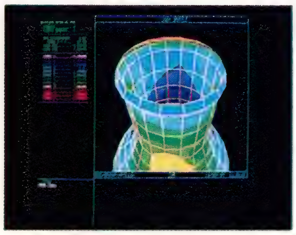


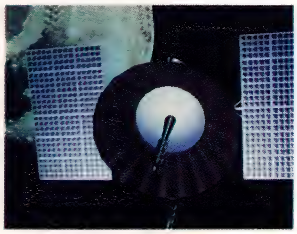
Multi-window industrial design

Computer-aided engineering and design

Industrial design



Structural analysis using finite element analysis



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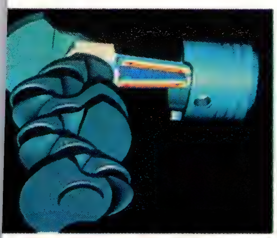

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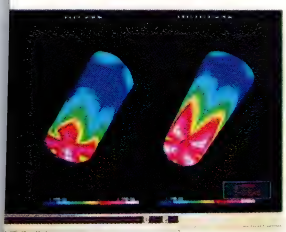
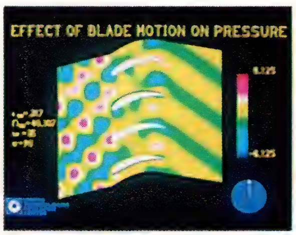
Automotive engineering

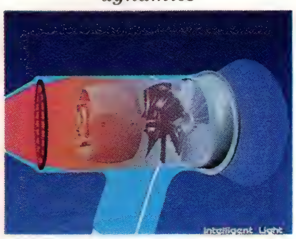
Computational fluid dynamics



Thermal analysis

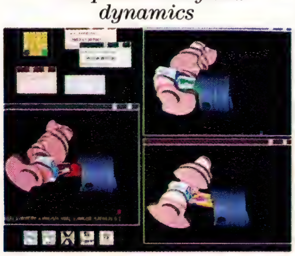


Computational fluid dynamics

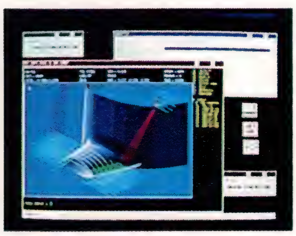


Industrial design

Industrial design



Computer-aided engineering



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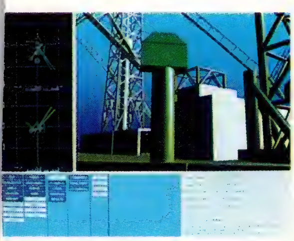
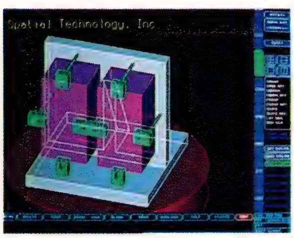


Scientific visualization



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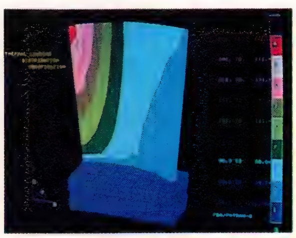

Finite element analysis

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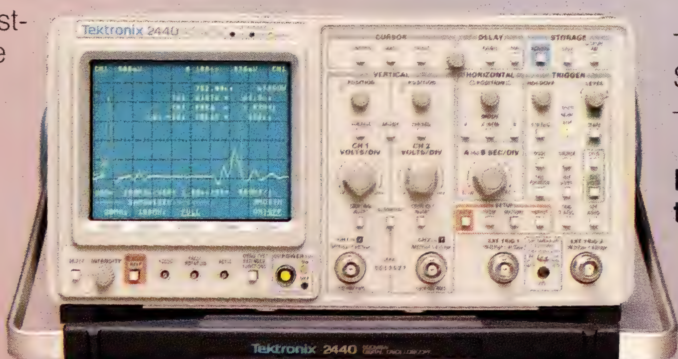

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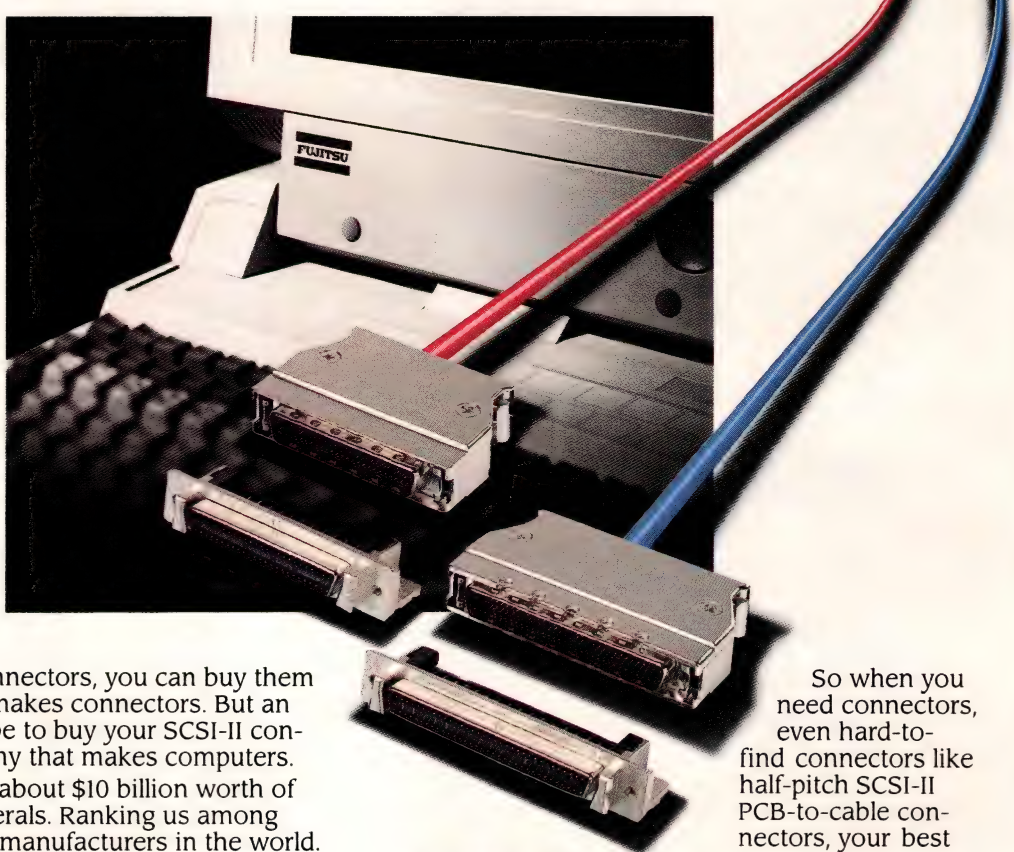
Why your best choice for SCSI-II connectors may not be a connector company at all.



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FCN-230 Series Connectors

Item	Specifications
Operating Temperature	–55°C to +105°C
Current Rating	1 ADC
Voltage Rating	240VAC
Contact Resistance	30mΩ max. at 6VDC, 0.1A
Insulation Resistance	1000MΩ min. at 500VDC
Dielectric Strength	750VAC for 1 minute
No. of Contact	50, 68

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Verification testers ease ASIC development

The role of ASIC verification testers has been reduced by high-quality simulation. However, these tools can still help you smooth the ASIC development cycle.

Doug Conner,
Regional Editor

Although the need for ASIC verification testers hasn't grown as rapidly as was predicted five years ago, the devices may have a place in your ASIC development process. The fact that the testers have not become prevalent is due, in large measure, to the advent of high-quality simulators. To understand how verification testers fit or don't fit into your ASIC development scheme, you must be aware of their benefits and drawbacks while you consider the entire ASIC development process. Problems in the ASIC development process generally spring from one of four sources: determining requirements, simulation, fabrication defects, and testing.

The majority of defective ASIC designs stem from problems in the requirements phase. Specifically, your ASIC is inadequately or improperly defined. If your design requirements aren't solidified, they may change while the ASIC is in development. Although a verification tester and the eventual target system itself can uncover such problems, both methods are undesirable because you will have already spent the time and money necessary to fabricate the ASIC. Whereas verification testing is limited to device pins, simulation can examine any node in an ASIC. Therefore, thorough simulation, perhaps including board-level simulation, is the best way to uncover such problems.

The majority of simulation errors occur because of incomplete simulation, and verification test programs are usually developed from simulation test vectors. Therefore, verification testers seldom find problems that can't be discovered using simulation.

Another source of simulation errors is the simulation itself, which usually means errors in the models, such as faulty transistors, used in the simulation. Because these errors are caused by the simulation, simulation can't uncover them. Fortunately, such errors are uncommon. In standard gate-array developments the likelihood of running into a model error problem is near zero. However, in a high-performance custom design the chance of a model error is more likely. There are more variables to be considered in custom design, and performance demands usually mean that foundries must push models closer to their limits.

Depending on the nature of the

The 50-MHz clock and data-rate tester *from Tektronix supports up to 256 I/O channels.*

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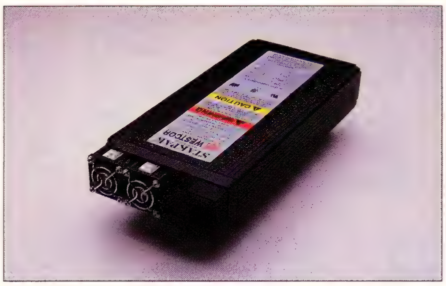
STAKPAK II STANDARD 600 WATT MODELS



Total output power may not exceed 600 watts for any model, single or multiple output. Lower power StakPak II models and many other configurations are available. Please contact the factory.

Model	Output Voltage (VDC) and Maximum Current (amperes) per Channel #1	#2	#3	#4	#5
Single Output					
ST1-1401	2 @ 120				
ST1-1402	5 @ 120				
ST1-1301	12 @ 50				
ST1-1302	15 @ 40				
ST1-1303	24 @ 25				
ST1-1304	28 @ 21				
ST1-1305	48 @ 13				
Dual Output					
ST2-1401	2 @ 60	5 @ 60			
ST2-1402	5 @ 60	5 @ 60			
ST2-1403	5 @ 60	12 @ 33			
ST2-1404	12 @ 33	12 @ 33			
ST2-1405	15 @ 26	15 @ 26			
Triple Output					
ST3-1401	5 @ 60	12 @ 16	12 @ 16		
ST3-1402	5 @ 60	15 @ 13	15 @ 13		
ST3-1501	5 @ 90	12 @ 8	12 @ 8		
Quad Output					
ST4-1401	5 @ 30	12 @ 16	12 @ 16	5 @ 30	
ST4-1402	5 @ 30	15 @ 13	15 @ 13	5 @ 30	
ST4-1403	5 @ 30	12 @ 16	12 @ 16	24 @ 8	
ST4-1501	5 @ 30	15 @ 13	15 @ 13	24 @ 8	
ST4-1502	5 @ 60	12 @ 16	12 @ 8	5 @ 15	
ST4-1503	5 @ 60	15 @ 13	15 @ 7	5 @ 15	
ST4-1504	5 @ 60	12 @ 16	12 @ 8	24 @ 4	
ST4-1505	5 @ 60	15 @ 13	15 @ 7	24 @ 4	
Five Output					
ST5-1501	5 @ 30	12 @ 16	12 @ 16	5 @ 15	24 @ 4
ST5-1502	5 @ 30	15 @ 13	15 @ 13	5 @ 15	24 @ 4

CIRCLE NO 50

STAKPAK STANDARD 1200 WATT MODELS

Total output power may not exceed 1200 watts for any model, single or multiple output. Lower power StakPak models and many other configurations are available. Please contact the factory.

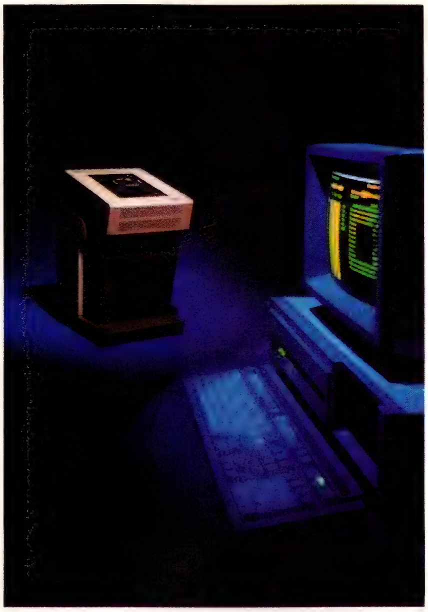
Model	Output Voltage (VDC) and Maximum Current (amperes) per Channel #1	#2	#3	#4	#5
Single Output					
SP1-1801	2 @ 240				
SP1-1802	5 @ 240				
SP1-1803	12 @ 100				
SP1-1604	15 @ 80				
SP1-1605	24 @ 50				
SP1-1606	28 @ 42				
SP1-1607	48 @ 25				
Dual Output					
SP2-1801	2 @ 120	5 @ 120			
SP2-1802	5 @ 120	5 @ 120			
SP2-1803	5 @ 120	12 @ 66			
SP2-1804	12 @ 66	12 @ 66			
SP2-1805	15 @ 53	15 @ 53			
Triple Output					
SP3-1801	5 @ 180	12 @ 16	12 @ 16		
SP3-1802	5 @ 150	12 @ 33	12 @ 16		
SP3-1803	5 @ 180	15 @ 13	15 @ 13		
SP3-1804	5 @ 150	15 @ 26	15 @ 13		
Quad Output					
SP4-1801	5 @ 150	12 @ 16	12 @ 16	5 @ 30	
SP4-1802	5 @ 150	15 @ 13	15 @ 13	5 @ 30	
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24 @ 8	
SP4-1804	5 @ 150	15 @ 13	15 @ 13	24 @ 8	
Five Output					
SP5-1801	5 @ 120	12 @ 16	12 @ 16	5 @ 30	24 @ 8
SP5-1802	5 @ 120	15 @ 13	15 @ 13	5 @ 30	24 @ 8
Seven Output					
SP7-1801	5 @ 60	12 @ 16	12 @ 16	24 @ 8	24 @ 8
	#6	#7			
	5.2 @ 28	2 @ 30			

ASIC verification testers

simulation error and the thoroughness of the foundry testing, a model error might be caught early on in the development scheme. If not, the error will not be caught until it reaches your actual target system. Here, verification testers are beneficial for two reasons: First, the ASIC prototype may be available before the circuit board it goes into is ready. Second, the verification tester provides a controlled environment that may be faster and better than your target system for evaluating the ASIC. Rather than just functionally testing the part in the circuit, an ASIC verifier can characterize the part and verify that it meets the original requirements.

Errors also occur during the actual fabrication process. Your design may be good, but a specific die may have a defect that prevents the ASIC from working properly. These problems are supposed to be caught by the foundry during its "production test"—a set of tests, agreed upon by the foundry and you, that defines what is a good part. Because testing can become a significant part of an ASIC's cost, and because some foundries don't have testers that can thoroughly test an ASIC at speed, compromises in production testing can let bad parts pass through the testing process.

A company that doesn't thoroughly test its ASICs at speed may find that the few defective ASICs that escape detection during production testing can be caught during system testing and replaced more economically than by using thorough production testing. This approach may cost less initially, but in the long run it guarantees increased quality problems by allowing inadequately tested parts to get into the field. If your system design uses a large number of ASICs, the probability of building in at least one defective ASIC in each system becomes too large, thereby mandating thorough production testing. If you don't plan to use thorough production testing, you should at least consider a thorough test of your engineering prototypes with a verification tester.



The XL series of testers *from IMS supports clock and data rates of 60 MHz and 100 MHz, respectively, with I/O channel counts of up to 448 or independent input and output channel counts of up to 896.*

The last problem source is the testing itself. Your ASIC (and the design) may or may not be defective, but something is causing the production test to fail. Because the foundry doesn't want to deliver the part until it has passed the production test, you don't get the part. Even if you smuggle one out of the foundry you won't have any confidence in the ASIC, nor will you be able to make any engineering decisions based on the ASIC.

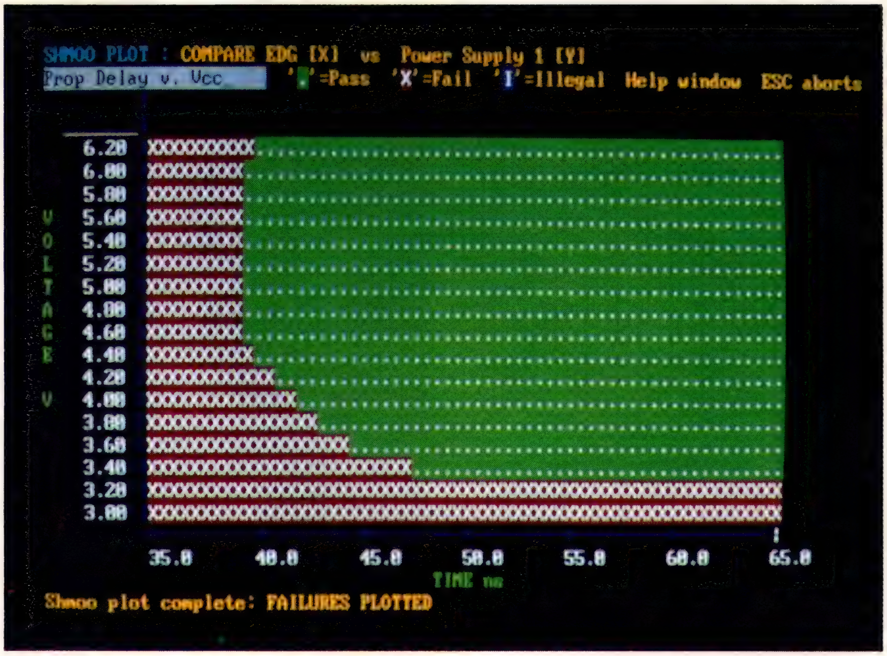
The usual way to resolve test errors is to get time on a tester to sort out the problems, whether the problem is as simple as an incorrectly wired board used to interface the ASIC to the test system, or an error in the test program. To solve test errors, the foundry usually needs an engineer from the customer company familiar with the design to help with the debugging. However, production testers are expensive and need to be used many hours a day to justify their cost. Since test-program debug time is often relegated to a few hours late at night, you can easily lose a week or more trying to correct problems you might find in one

The 200-MHz clock and data rate *HP82000 model D200 is available in a benchtop cabinet with up to 80 I/O channels or in a system rack with up to 384 I/O channels.*

ASIC verification testers

10-hour stint—if you can get time on the tester.

If you want to use a verification tester to help debug a test program, you must consider both the ability to correlate data between the verification and production testers and the ability to translate test programs easily between the two. Because verification-tester manufacturers realize the importance of being able to freely translate programs between a verification tester and a production tester, they have all made efforts to provide software to make the translations as simple as possible. It's probably best to consult the foundry or foundries you will be using to find out which production testers they will be using, and then see what level of support the verification-tester manufacturer can offer for those particular testers.



A voltage-versus-time plot *such as this one made with a Hilevel Topaz V shows how power-supply voltages affect device performance. Software that automates this function saves considerable time. Plots such as this are called "shmoo plots."*

You also need to provide software to translate the simulation test vectors into a verification test program. Verification-tester manufacturers support most of the popular formats, but if you use a proprietary simulator, you're in for some extra work. Once you get the test program into the verifier, you probably will want to add to the program. The software needs to be easy for the infrequent user to work with. Because what-if experiments are the rule rather than the exception when using verification testers, manufacturers have made verifiers easy for design engineers to use.

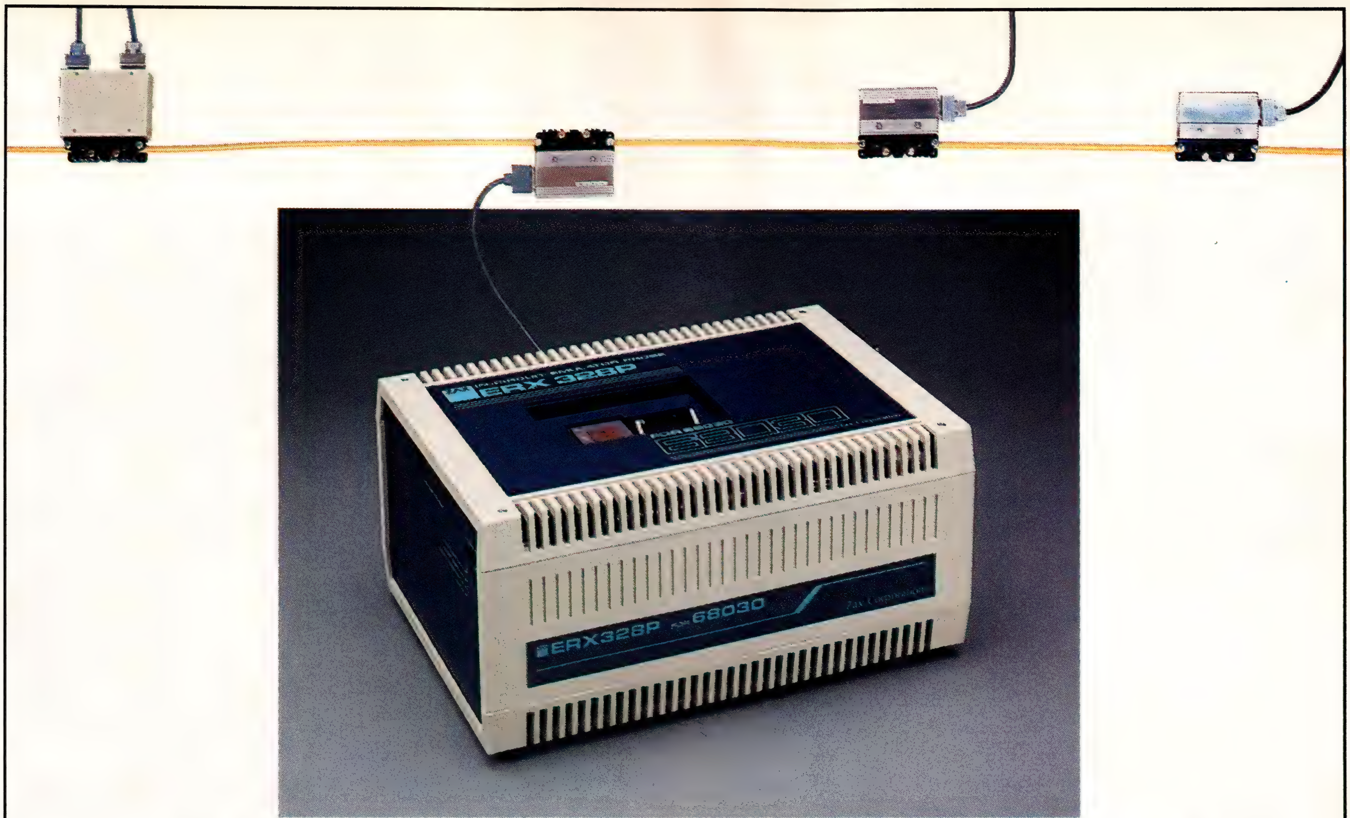
Testing an ASIC occurs on two levels—the functional level and the characterization level. During functional testing, you make sure the logic functions performed by the ASIC are correct. Timing, voltage levels, and current levels are set to values that won't challenge the ASIC's performance while functionally testing the logic. Functional testing also doesn't challenge the tester, whether it be a verification tester or a production tester.

Home brew for high performance

If you are developing high-performance ASICs with data rates above 100 MHz, your choices for ASIC verifiers (or production automatic test equipment (ATE)) are few. Above 200 MHz you won't find a stock solution. You could try functionally testing a 250-MHz part at 100 MHz and assume it will work at full speed in your target system, but you'd be following a well-worn path to a dead end. You can occasionally practice such a test philosophy on low-speed parts, but it won't work for high-performance applications.

One solution is to build your own tester from components. Outlook Technology (Campbell, CA (408)374-2990) supplies high-speed pattern generators and logic-analysis building blocks for those of you who build your own high-performance test systems. Systems built from these building blocks allow engineers to test ECL and GaAs devices that operate at speeds of 500 MHz and faster. Other sources for home-brew building blocks are standard high-performance logic-analyzer manufacturers.

These solutions aren't easy. You'll expend much effort maintaining signal integrity through the interface between the tester and the device. You'll also have to develop all the software yourself. But if you're after the highest performance, there is no easy solution.



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ASIC verification testers

Characterization testing, on the other hand, makes high demands on both verification testers and production testers. You perform characterization testing to gather detailed performance information on the ASIC, including timing margins and dc parametric tests. The test results show you whether or not the ASIC meets all of your original performance requirements.

System accuracy

Your test system must be accurate in order to accurately measure setup times, hold times, and propagation-delay times. **Table 1** lists the accuracy of a representative group of verification testers. The accuracy values listed are difficult to compare directly because it isn't clear whether each manufacturer is including all the system errors in its number. Accuracy is defined as the pin-to-pin skew across the entire test system.

Manufacturers measure skew under certain conditions of data format, rising or falling edges, voltage levels, and other parameters that may not necessarily be representative of your application. For example, setup-and-hold time measurements depend on the pattern-generator (stimulus) skew. Propagation measurements depend on pattern-generator skew and acquisition (compare) skew. You can spend time with a verification system's manufacturer to understand its system's accuracy; however, a better method is to use an accurate high-performance oscilloscope and make the measurements yourself.

Though accuracy is the cornerstone of any instrument used for measurements, you must meet other requirements for particular testing applications such as pin counts and data rates. **Table 1** lists several such requirements.

Depending on the device you are testing, test-vector memory can be an important consideration. As **Table 1** shows, there is considerable variation in the capacity of different testers. Because reloading the pattern memory can be time consuming, it's best to fit your entire set of test vectors in memory. One feature that helps you compress larger sets of test vectors into a small amount of memory allows looping and branching in the test program. Depending on how many times you repeat a subset of your test vectors, looping and branching can make up for a considerable amount of test-vector memory.

***The System 6000** from Gould supports up to 352 I/O channels with 25-MHz data rates and 50-MHz clock rates.*

A second key memory-related variable is scan-path testing. The various methods of scan testing require large amounts of test vectors behind one or perhaps a few pins. Addressing this problem, some verification testers offer the flexibility to use memory that is not equally divided behind each pin. Rather, the desired scan pins are assigned large blocks of memory.

Two terms you'll often hear concerning testers are per-pin and shared-resource architectures. Every high-performance verification tester is said to have a per-pin architecture. In reality, they are all combinations of per-pin and shared-resource architectures. The per-pin label refers to a tester-per-pin, whereby each pin is treated independently of all the other pins. Shared-resource architecture, as the name implies, means that resources are shared between multiple pins.

To illustrate the difference, consider timing generators, which can use either architecture. A timing generator supplies timing edges used to control data and events for each pin on the tester. The format data determines what happens at each timing edge. In a per-pin timing-generator architecture, such as Hewlett-Packard's 82000 systems, each pin has two timing edges that can be placed within a timing cycle, independently of other pins. In a shared architecture, a number of timing generators are available, typically between six and 16, with each timing generator supporting two edges. Each channel must use the timing available from one of the timing generators.

Text continued

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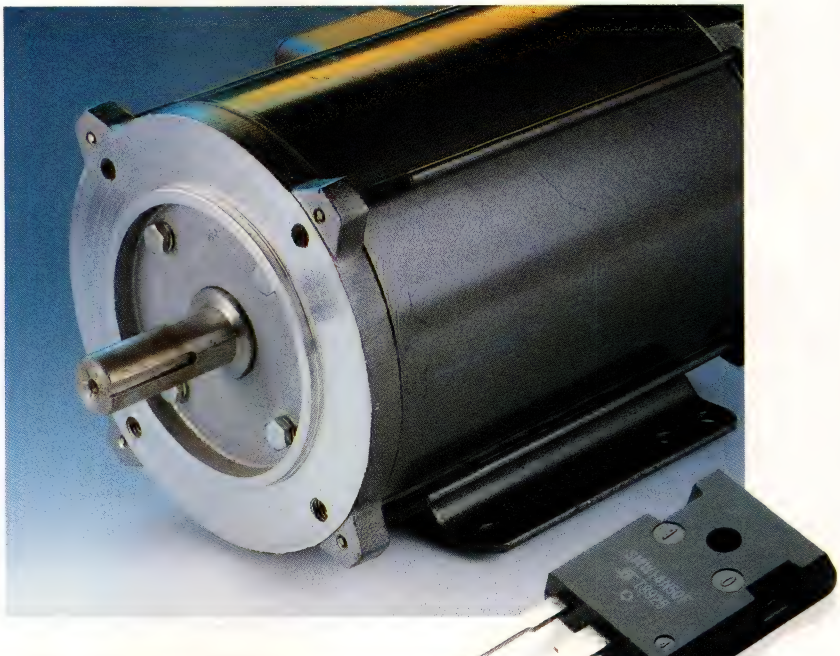

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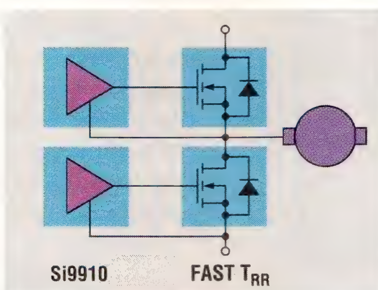

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TABLE 1—REPRESENTATIVE ASIC VERIFICATION TESTERS

MANUFACTURER	MODEL	I/O CHANNELS MINIMUM	I/O CHANNELS MAXIMUM	MAXIMUM DATA RATE (MHz)	MAXIMUM CLOCK RATE (MHz)	TIMING ACCURACY (± pSEC)	TIMING RESOLUTION (pSEC)
ASIX	ASIX 1	128	256	25/50	100	1000	100
GOULD	SYSTEM 6000	64	352	25	50	3000	1000
HEWLETT-PACKARD	8200 D50	48	512	50	50	500	200
	82000 D200	24	384	200	200	250	50
HILEVEL	TOPAZ FX	18	224	30	60	1500	500
	TOPAZ VL	32	256	50	50	1000	100
	TOPAZ V320	32	320	110	110	500	100
	TOPAZ V544	32	544	110	110	500	100
IMS	XL-60	16	224	60	60	1000	100
	XL-100	16	224	100	100	1000	100
	XL-2	16	448	60/100	60/100	1750	100
TEKTRONIX	LV500	64	256	50	50	2000	500

NOTE:
*=VIRTUAL VECTOR MEMORY
66k WORDS FOR 320 CHANNELS
463k WORDS FOR 32 CHANNELS

TIMING-GENERATOR EDGES	TEST-VECTOR MEMORY (k WORDS) STANDARD	TEST-VECTOR MEMORY (k WORDS) OPTIONAL	TEST PATTERN LOOPING & BRANCHING	SCAN-TESTING SUPPORT	PARAMETRIC MEASUREMENT UNIT	SOFTWARE FIXTURING	PRICE
3 PAIRS & 3 PAIRS (OPTIONAL)	16	64	✓	OPTIONAL	✓	✓	$500/PIN
8	16	64	LOOPING ONLY	—	OPTIONAL	✓	$38,000-$129,000
2 PER PIN	64	256	✓	✓	OPTIONAL	✓	$240,000 (256 CHANNELS)
2 PER PIN	128	—	✓	✓	OPTIONAL	✓	$193,000 (64 CHANNELS)
16	4	16	✓	OPTIONAL	—	—	$400-$450/PIN
16	*	—	✓	✓	OPTIONAL	✓	$800-$900/PIN
16	*	—	✓	✓	OPTIONAL	✓	$1000-$1200/PIN
16	*	—	✓	✓	OPTIONAL	✓	$1200-$1300/PIN
12 PAIRS	16	64	✓	OPTIONAL	OPTIONAL	✓	$55,000-$250,000
12 PAIRS	16	64	✓	OPTIONAL	OPTIONAL	✓	$70,000-$400,000
12 PAIRS	16	64	✓	OPTIONAL	OPTIONAL	✓	$450,000-$800,000
16 PAIRS	64	—	✓	—	FUTURE OPTION	✓	$55,000-$172,000

ASIC verification testers

The problem with shared-resource architecture is not that you will run out of resources, although that is possible. Rather, it is the lack of flexibility you have to develop and alter your test programs. Globally shared resources, whereby any pin can use any timing generator, are not too constraining. However, when you have locally shared resources (a specific timing generator can only be used by a subset of the pins), the constraints can reduce tester flexibility and add complexity to the software.

Timing generators are only one in a long list of features that can be either a per-pin or a shared resource. All high-performance verification systems use at least a limited set of per-pin features so that they can have what is often called software fixturing. To simplify the test fixturing of devices, fixtures are built for each package type so that each pin on the device is routed to a pin on the tester. Therefore, only power pins must be custom wired for testing a particular device.

The reason a per-pin architecture is required for software fixturing is that you need total flexibility in the system because each device will use pins differently. For example, you need independent control on each pin to select whether that pin will be an input or output. If the input/output select is switched in banks of eight pins, software fixturing won't work.

Many verification testers provide an optional parametric measurement unit (PMU) to perform dc voltage and current measurements on device pins. The PMU is used for checking continuity to pins, drive capability, leakage, and many other measurements useful in characterizing a device.

Unlike most equipment that design engineers use, verification testers often require more support both before and after the sale. If you're seriously considering the purchase of a verification tester but have concerns about the capability of a particular tester to meet your needs, the best approach is often to have the vendor test one of your parts. Let them show you that their tester can perform to meet your needs; at the same time you can see just how easy (or difficult) the software is to use on a real problem.

When trying to assess the applicability of a verification tester to your ASIC development process, there is another way to view the problem. You have an ASIC prototype that passes the foundry's test program and it works in your prototype system. Are you comfortable about releasing the part to volume manufacturing, or would you like to perform more characterization tests on the device? If you choose the latter, you should consider a verification tester. EDN

Article Interest Quotient
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For more information . . .

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Fremont, CA 94538
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FAX 415-656-8245
Circle No 710

Gould Inc, Test and Measurement
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Cupertino, CA 95014
(408) 988-6800
FAX 408-988-1647
Circle No 711

Hewlett-Packard Co
Box 10301
Palo Alto, CA 94303
Phone local office
Circle No 712

Hilevel Technology Inc
31 Technology Drive
Irvine, CA 92718
(714) 727-2100
FAX 714-727-2101
Circle No 713

Integrated Measurement Systems Inc
9525 SW Gemini Drive
Beaverton, OR 97005
(503) 626-7117
FAX 503-644-6969
Circle No 714

Tektronix Inc
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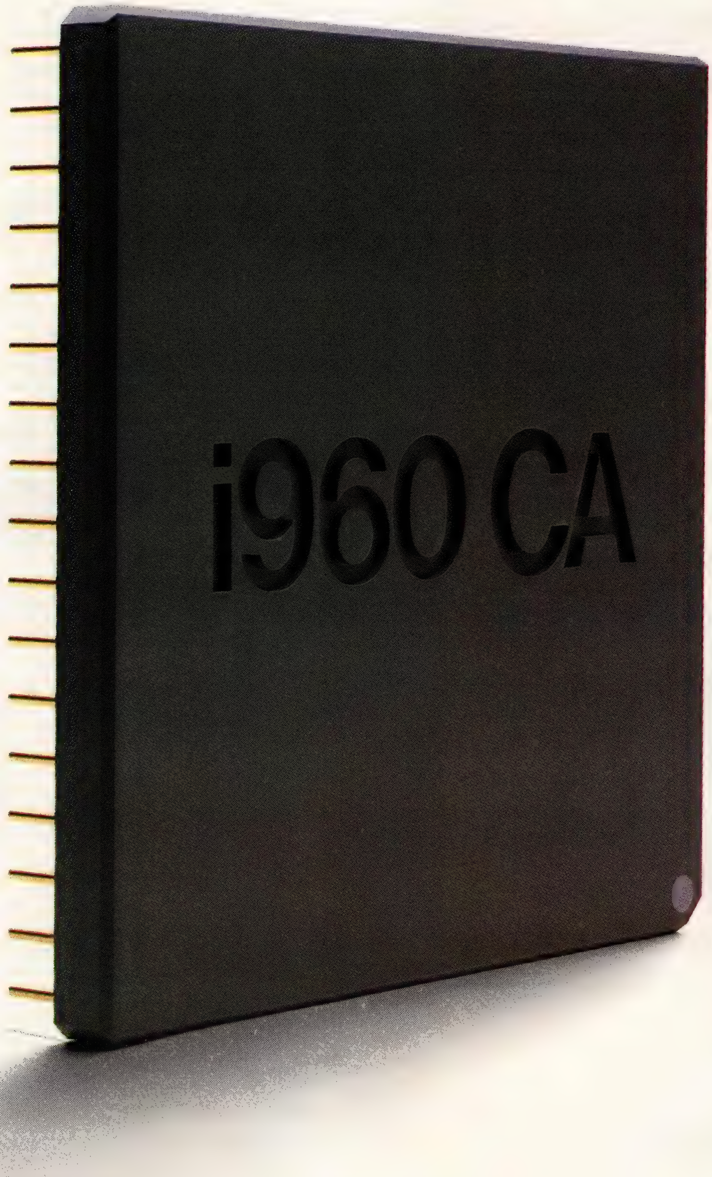
WHAT'S COMING IN EDN

EDN Magazine's December 7, 1989, issue is the first installment of our December Product Showcase. It will contain staff-written articles and product reviews in four key technology areas:

- Hardware and Interconnect Devices
- Integrated Circuits
- Power Supplies
- Software.

Also look for our regular departments. The second December Product Showcase will cover Components, Instruments, Computers and Peripherals, and Computer-Aided Engineering.

Multiple instructions per clock is not a barrier.



National Semiconductor

Our 32CG16 processor made quite a name for itself.

EDN's 16th Annual μP/μC Chip Directory

Michael C Markowitz,
Associate Editor

As ICs' feature sizes shrink with improvements in process technology, chip vendors have three alternatives: They can make the same chip on a smaller die, add features to the CPU to give the chip greater processing power, or add peripheral circuitry to the CPU that would normally be external to the processor.

General-purpose μPs and μCs are losing their general-purpose nature as vendors use available chip space to tailor a chip's periphery for specific applications.

Of the three alternatives, many vendors are coming to realize that getting a CPU with the *right* combination of peripherals provides you with the greatest benefit. After all, a cheaper μP or μC will save you some money, but compatibility and packaging constraints limit the vendor's ability to change packages. However, if the vendor uses the same package, you won't save board space. And, although it's always nice to have more processing power, if you really needed more power, you'd have chosen a more powerful CPU to begin with. By moving peripheral circuitry onto the processor IC, you can eliminate chips from your board, thus giving you three alternatives: You can make the same circuit on a smaller board, add features to the system to give it greater capability, or use the same board and add chips from other boards in the system to improve performance and maybe even eliminate boards.

But what are the *right* peripherals? Obviously, you'd need different peripherals for a flight controller than you would if your circuit were going into a communications system. Additionally, you'd probably want some assurance that the ICs on your flight-controller board would function under the conditions the board is likely to encounter. If your design requirements are less critical, you wouldn't want to pay for features and capabilities that you won't use.

One way to get only the processor and the peripherals you need on your μP or μC is to build an ASIC. Unfortunately, you'll need relatively high volumes for this strat-

μP and μC chips shatter conventions by finding their way into ubiquitous applications, such as planes, trains, and automobiles; toys; fax machines; and audio and video equipment. (Photo courtesy Intel)


Handycam PRO

If you're really lucky, an insightful marketing maven will have anticipated your µC needs.

egy to be cost effective. Further, a plethora of CAD tools are available to simplify the hardware design of your ASIC, but unless you provide access to the ASIC's µP core, commercially available development tools won't help you much with the software design.

Another way to get the right peripherals is to buy one of the application-specific µCs that companies such as Hitachi, National Semiconductor, Toshiba, and Zilog offer. These companies put a particular assortment of peripherals around a µP core and target specific applications. Unfortunately, MBA types decide which markets to target application-specific µCs for. And, as is often the case, marketing decisions don't always make an engineer's life any simpler. If you're designing a box for an industrial control system and application-specific µPs and µCs exist, you can start your search there. But, a vendor's claim that its µP or µC targets an application that doesn't correlate to your needs shouldn't necessarily eliminate that IC from consideration.

Consider, for example, the Motorola 68332, which is based on the 32-bit 68020. The µC features a clock-generator module that contains a PLL. The PLL enables the µC to operate at 16.78 MHz from a 32.768-kHz crystal, which keeps costs down and minimizes system RFI. The controller also offers a CPU-independent, microcoded, time processing unit that performs 12 preprogrammed functions, such as measuring frequency and pulse width.

Although Motorola designed the 68332 as an automotive µC to perform engine control tasks, that definition shouldn't restrict its use. If you design circuits for robotics, high-performance control systems, or any other time-intensive application, you might also be able to make use of the µC's time processing unit.

Familiar cores accept standard code

Like the 68332, application-specific processors generally use familiar cores, although unlike the 68332, most use 4-, 8-, and 16-bit cores. Improvements and application-specific enhancements have helped prolong the lives of many small-bus-width processor families, such as the 6800, 8051, and Z80. There are three reasons popular small cores often serve as the base for these µCs. First, and perhaps most important in embedded applications, is cost. In addition to the CPU costing less, small-bus-width µPs and µCs require fewer memory chips; less glue logic; and, consequently, less board space. These savings can be substantial.

A second advantage to using familiar µPs and µCs is that you can port code to them from older designs. Reusing code can save you time and improve your chances of getting bug-free software. And, with most of the older standard µPs and µCs, you have a wealth of available code.

The third consideration is density. You can only fit so much on an IC, and although current transistor-count limits will let you put a 32-bit µP on an integrated circuit, you can't fit much more. In fact, Roger Ross, president and chief executive officer of Ross Technologies (Austin, TX) and head of the design team of the Motorola 88000, salivates in anticipation of the day when he can build a 32-bit RISC (reduced-instruction-set computer) chip with two to three million transistors. Only then could he integrate all the right peripherals around the core CPU. Ross's dream chip would include an integer unit, a memory-management unit, a floating-point unit, a cache controller, and 32k bytes of cache memory on one manufacturable piece of silicon.

However, in spite of the media's coverage of high-end glamour processors like the 80486, i860, 68040, and SPARC, most designers are still working with 4-and 8-bit µPs and µCs. (According to Dataquest, a market-research firm in San Jose, CA, 4- and 8-bit µPs and µCs accounted for 99% of the 1988 total µP and µC unit volume.) There is a good reason for working with the lower-bit-density µPs and µCs.

As discussed in last year's directory **(Ref 1)**, the embedded-control market consumes the greatest number of µPs and µCs. These invisible processors compete in an extremely price-sensitive arena where an extra nibble or byte could make your system too expensive to sell. Therefore, cost constraints limit your ability to over-design your circuit and still stay competitive. Also, your investment in code presents a certain inertia that restricts your ability to change µP or µC families.

But, if embedded systems are so price sensitive, where do RISC processors fit in? According to a few vendors of CISC-based (complex-instruction-set computer) µPs and µCs, RISC µPs fit only at the highest end of the performance spectrum, where you absolutely, positively can't live without the performance gain that RISC is supposed to provide. These vendors

concede the high-end market to RISC-based processors. Russ Johnson, director of imaging and graphics products at National Semiconductor, points to applications such as MIS (management information systems) printers costing upwards of $200,000 and other expensive systems where the CPU is only a small part of the total cost as potential application areas for RISC processors. Others, like Wayne Ricardi, vice president of marketing and sales at Zilog, make no such concession. They believe that the power of smaller distributed-computing processors can free up the central CPU. Ricardi grants RISC-based μCs an edge at crunching numbers, but claims that their cost and generally poor ability to perform control functions with the calculated results argues against their use in embedded-control systems.

Is RISC a fad?

Jack Ganssle, president of Softaid (Columbia, MD), a development-tool vendor, represents a third camp. Although he might justify using RISC-based controllers in fly-by-wire jets and for redundant processors in critical applications, he wouldn't choose a RISC-based μC over a CISC-based one. Ganssle likes RISC's single-cycle execution of common instructions and the optimizing compilers that keep a RISC μP's pipeline full, but he suggests that RISC is just the latest fad. He believes that engineers who want to play with the latest and greatest μPs and μCs are choosing RISC chips because of RISC's glamour and because design decisions are being made at too low a level. Ultimately, Ganssle expects CISC chips to win out because of the volume of existing code for them and their hardware advantages. He predicts that future incarnations of CISC chips will incorporate most of the positive features of RISC technology into CISC-based processors and controllers, as we've started to see already.

On the other hand, Rick Rasmussen, director of market development for LSI Logic, argues that RISC-based embedded-control systems were more expensive a year ago. Today, however, RISC chips are speeding down the learning and cost curves, and there is a rough parity between RISC- and CISC-based controllers. Rasmussen claims that RISC-based μPs are suitable for a wide range of applications, such as laser printers, LAN controllers, and real-time interrupt controllers. In light of these comments, you won't be surprised to learn that LSI Logic is pursuing the application-specific μP/μC strategy with two RISC-based processors: one with a SPARC core and the other with the Mips core. And, although Rasmussen doesn't dispute that the bulk of current design work uses 4- and 8-bit machines, he's convinced that, despite significantly higher costs, designers will be using 16- and 32-bit μPs and μCs in a growing percentage of future designs.

Roger Ross, the president of Ross Technologies, is

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	120	Z8, Super8
	122	7000
	124	8085H/80C85
	126	Z80
	128	HD 64180/Z180
	130	6800/6802, 6809/6309
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	138	8086/8088
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	169	68000 family
	170	SERIES 32000
	171	VL 86C0X0
	172	80386
	173	80486
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	175	SPARC RISC
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	180	29000 RISC
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	183	80960
	184	i860
Building block families	185	2900 Bit Slice
	186	29300/400, 29C300
	190	74AS8XX/74AS88XX
	192	Word Slice

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TLX 82772977
Circle No. 653

Bipolar Integrated Technology
1050 NW Compton Dr
Beaverton, OR 97006
(503) 629-5490
FAX 503-690-1498
Circle No. 654

California Micro Devices
2000 W 14th St
Tempe, AZ 85281
(602) 968-4431
FAX 602-921-6298
Circle No. 655

Calmos Products Div
(Recently acquired by
Newbridge Microsystems)
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Kanata, Ontario, Canada K2L 1V8
(613) 836-1014
FAX 613-831-1742
Circle No. 656

Cypress Semiconductor
3901 N First St
San Jose, CA 95134
(408) 943-2902
FAX 408-943-2741
Circle No. 657

Dallas Semiconductor
4350 Beltwood Pkwy
Dallas, TX 75244
(214) 450-0400
FAX 214-450-0470
Circle No. 658

Eurosil Electronic GmbH
Erfurter Str 16
8057 Eching
West Germany
49-89-31906-128
FAX 49-89-319-462-1
Circle No. 659

Fujitsu Microelectronics Inc
3330 Scott Blvd
Santa Clara, CA 95054
(408) 727-1700
FAX 408-922-9128
Circle No. 660

Gould Semiconductor (AMI)
2300 Buckskin Rd
Pocatello, ID 83201
(208) 233-4690
Circle No. 661

Harris
Semiconductor Products Div
Box 883
Melbourne, FL 32902
(407) 724-7418
FAX 407-729-5691
Circle No. 662

Hitachi America Ltd
2000 Sierra Point Pkwy
Brisbane, CA 94005
(415) 589-8300
FAX 415-583-4207
Circle No. 663

Hitachi Ltd
Semiconductor &
Integrated Circuits Div
New Marunouchi Bldg 5-1
Marunouchi 1-Chome
Chiyoda-ku, Tokyo 100, Japan
(03) 212-1111
Circle No. 664

Ingenieurbüro Otto Müller
AM Guckenbühl 10
7750 Konstanz 16
0-75-31-432-12
FAX 0-75-31-517-25
Circle No. 665

Inmos Corp
(Recently acquired by SGS-Thomson)
Box 16000
Colorado Springs, CO 80935
(719) 630-4000
TLX 62944936
Circle No. 666

Inmos Ltd
(Recently acquired by SGS-Thomson)
1000 Aztec W
Almondsbury
Bristol BS12 4SQ, UK
(0454) 616616
Circle No. 667

Integrated Device Technology
3236 Scott Blvd
Santa Clara, CA 95051
(408) 727-6116
Circle No. 668

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
(408) 987-8080
Circle No. 669

Intel Corp
Embedded Processor Group
5000 W Chandler Blvd
Chandler, AZ 85226
(602) 554-8080
Circle No. 670

Intergraph Corp
Advanced Processor Div
2400 Geng Rd
Palo Alto, CA 94303
(415) 494-8800
FAX 415-856-9224
Circle No. 671

Intermetall GmbH (ITT)
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D-7800 Freiburg, West Germany
(0761) 5170
Circle No. 672

LSI Logic Corp
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Milpitas, CA 95035
(408) 433-8000
FAX 408-433-7447
Circle No. 673

Microchip Technology
2355 W Chandler Blvd
Chandler, AZ 85224
(602) 345-3287
Circle No. 674

Mitsubishi Electronics America Inc
1050 E Arques Ave
Sunnyvale, CA 94086
(408) 730-5900
FAX 408-720-0429
Circle No. 675

Motorola Integrated Circuits Div
3501 Ed Bluestein Blvd
Austin, TX 78721
(512) 928-6000
Circle No. 676

Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
(512) 440-2000
Circle No. 677

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
(408) 721-5000
FAX 408-730-0764
Circle No. 678

NCR Corp
2001 Danfield Ct
Fort Collins, CO 80525
(303) 226-9500
Circle No. 679

NCR Microelectronics Div
1635 Aeroplaza Dr
Colorado Springs, CO 80916
(719) 596-5612
Circle No. 680

NEC Electronics USA Inc
(US Headquarters)
401 Ellis St
Mountain View, CA 94039
(415) 960-6000
Circle No. 681

NEC Electronics USA Inc
Microcomputer Div
1 Natick Executive Park
Natick, MA 01760
(508) 655-8833
FAX 508-872-8692
Circle No. 682

NV Philips
Eindhoven, The Netherlands
31-40-79-3333
Circle No. 683

Oki Semiconductor Inc
650 N Mary Ave
Sunnyvale, CA 94086
(408) 720-1900
Circle No. 684

Panasonic (Matsushita)
2 Panasonic Way
Secaucus, NJ 07094
(201) 348-5217
FAX 201-392-4652
Circle No. 685

Rockwell International Corp
Semiconductor Products Div
Box C
4311 Jamboree Rd
Newport Beach, CA 92658
(714) 833-4700
Circle No. 686

Seeq Technology Inc
1849 Fortune Dr
San Jose, CA 95131
(408) 432-9550
Circle No. 687

SGS-Thomson Microelectronics
Via C Olivetti 2
20041 Agrate Brianza, Italy
(3939) 6555590
Circle No. 688

SGS-Thomson Microelectronics Inc
1000 E Bell Rd
Phoenix, AZ 85002
(602) 867-6259
Circle No. 689

Sharp Corp
Integrated Circuits Group
2613-1, Ichinomoto-Cho, Tenri-shi
Nara 632, Japan
Circle No. 690

Sharp Microelectronics Corp
Box 650
Mahwah, NJ 07430
(201) 529-8757
Circle No. 691

Siemens AG Semiconductor Div
Balanstrasse 73
Postfach 80 17 09
8000 Munich 80
West Germany
49-89-4144-8271
FAX 49-89-4144-3979
Circle No. 692

Siemens Components Inc
Semiconductor Group
2191 Laurelwood Rd
Santa Clara, CA 95054
(408) 980-4500
FAX 408-980-4529
Circle No. 693

Sierra Semiconductor
2075 N Capitol Ave
San Jose, CA 95132
(408) 263-9300
Circle No. 694

Signetics (Philips Components)
811 E Arques Ave
MS 76
Sunnyvale, CA 94088
(408) 991-2000
FAX 408-991-2311
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Standard Microsystems Corp
35 Marcus Blvd
Hauppauge, NY 11788
(516) 273-3100
FAX 516-273-3123
Circle No. 696

Texas Instruments Inc
MOS Microcomputers
Box 1443
Houston, TX 77001
(713) 274-2000
FAX 713-274-2445
Circle No. 697

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Microprocessor and
Microcontroller Products Div
Box 809066
Dallas, TX 75380
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Circle No. 698

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Colorado Springs, CO 80907
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Camarillo, CA 93010
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FAX 805-987-5896
Circle No. 701

VLSI Technology Inc
8375 S River Pkwy
Tempe, AZ 85274
(602) 752-8574
FAX 602-752-6000
Circle No. 702

WaferScale Integration Inc
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Fremont, CA 94538
(415) 656-5400
Circle No. 703

Weitek Corp
1060 E Arques Ave
Sunnyvale, CA 94086
(408) 738-8400
Circle No. 704

Western Design Center Inc
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Mesa, AZ 85203
(602) 962-4545
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Campbell, CA 95008
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High Interest 470 **Medium Interest 471** **Low Interest 472**

a strong supporter of RISC technology. Ross will concede the low-end embedded-control applications to CISC-based µCs—for now. And although he also concedes that today's RISC technology is still more expensive than CISC, he says that there is nothing inherently more costly about RISC. Still, he insists that given equal transistor counts, RISC offers two-and-a-half to three times the performance of CISC. Ross thinks the question is, do you build a laser printer for less than $1000 with CISC technology, or do you maximize performance with RISC? In addition, Ross claims that embedded-control designers aren't as sensitive to using pre-existing code as other vendors might claim. Rather, the important issues for designers are whether the µP has a decent compiler and whether the price/performance ratio is appropriate for their application. EDN

Reference

1. Titus, Jon, "EDN's 15th Annual µP/µC Chip Directory," *EDN*, October 27, 1988, pg 164.

Note

With the large number of µPs and µCs introduced every year, it is impossible to give you a comprehensive listing of every available device. This year's directory provides "bingo" numbers in the listings primarily to let you request information about the processors, but also to let us see where your interests lie. If there are other µP or µCs, new or old, that you'd like to see covered, let us know; jot the part number down on the bingo card, send us a letter, or give us a call.

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

COP400

4-BIT NMOS AND CMOS

AVAILABILITY: Now.
COST: Under $0.50 for NMOS 413L and under $1 for CMOS 413C in very high volume (1M/yr).
SECOND SOURCE: Thomson (over 6M units in 1986).
CORE: Core μP concept has been used all along for this single-chip family, although on an internal basis.

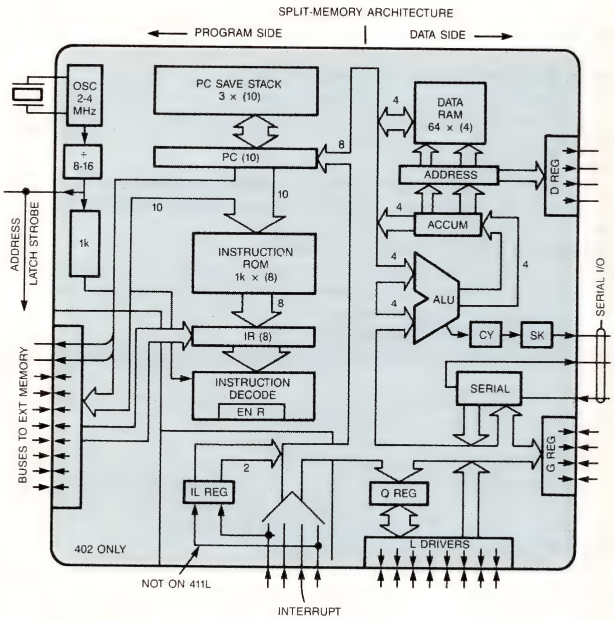
Description: NMOS and CMOS minimum-cost single-chip family. COP chips are microcontrollers intended to make low-cost, intelligent products feasible, and contain the complete μC system—μP, memory, and I/O—necessary to implement dedicated control functions. Typical application would be as lone chip in a low-cost toy for mass consumer market, where it would provide the intelligence to interface to a human.

National Semiconductor Corp
2900 Semiconductor Dr, MS 16-174
Santa Clara, CA 95051
Phone (408) 721-5000

For more information, Circle No. 720

Status: Note that National's COP800 (next entry) is similar to COP400 in name only; it has a different architecture and instruction set.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. ROMless 402 and 404 are available for development and low-volume production, as well as piggyback CPUs that carry standard EPROMs.
2. Some COP400 models and peripherals are configured with National Microbus serial I/O for easy exchange of data with low pin count.
3. CMOS chips have optional multi-input wake-up feature, improved timer, and interrupt-on-overflow. All CMOS chips designed for increased ESD and latch-up margin.
4. 24- and 28-pin surface-mount packaging available for space-sensitive applications, such as consumer goods.

COP400 FAMILY (CMOS MEMBERS)

PART NUMBER	MEMORY ROM (BYTES)	MEMORY RAM (DIGITS)	I/O PINS	INTERRUPT	STACK	TIMER BASE COUNTER	SIZE (PINS)	OTHER
COP413C	0.5k	32	16	NO	2 LEVEL	NO	20	
COP413CH	0.5k	32	16	NO	2 LEVEL	NO	20	
COP410C	0.5k	32	19	NO	2 LEVEL	NO	24	
COP411C	0.5k	32	16	NO	2 LEVEL	NO	20	
COP424C	1.0k	64	23	1 SOURCE	3 LEVEL	YES	28	PMP
COP425C	1.0k	64	20	NO	3 LEVEL	YES	24	PMP
COP426C	1.0k	64	16	NO	3 LEVEL	YES	20	PMP
COP444C	2.0k	128	23	1 SOURCE	3 LEVEL	YES	28	PMP
COP445C	2.0k	128	20	NO	3 LEVEL	YES	24	PMP

NOTE: PMP IS POST-METAL PROGRAMMING.

I—DATA-MANIPULATION INSTRUCTIONS
Binary arithmetic with BCD handled by add immediate. Only logical function is exclusive-OR. Can test individual bits in RAM.
II—DATA-MOVEMENT INSTRUCTIONS
Direct and indirect movements between data RAM and accumulator.
Like some other 4-bit, 1-chip μCs, makes use of built-in exclusive-OR in instruction to flip back and forth between nibbles of data strings.
Combination instructions permit indexing forward and backward through data RAM.
Move 8-bit pattern from instruction ROM to Q output register, also 8-bit table look-up on input.
Can set up operating modes on serial I/O with software, turning chip into counter if desired.
I/O instructions to individually serve unique I/O ports.
III—PROGRAM-MANIPULATION INSTR
Jump and jump indirect.
Jump and return from subroutine (three levels of return stack; two for 410L).
Skip-type conditional test instructions.
Vectored hardware interrupt.
IV—PROGRAM-STATUS-MANIP INSTR
Set and carry bit and interrupt enable (there's a means for saving carry status upon interrupts).
V—POWER-SAVING INSTRUCTIONS
Halt instruction disconnects internal circuitry from clock, which lowers power consumption to a few μA. Because chip is static CMOS, all registers retain data and upon Reset restart from where they left off.

Specification summary: Single-chip μC with split-memory architecture; 8-bit-wide instruction side (1k bits for 420 part) and 4-bit-wide data side (64 bits for 420 part). Considerable on-chip I/O despite small package size (28 pins for 420) including clocked serial/event-counter port. Family includes 30 devices with different memory and I/O options and is fabricated in several device technologies, including basic metal-gate NMOS and CMOS. Power for CMOS will vary from 3 mA at 14-μsec cycle to 120 μA with 64-μsec cycle (using 32-kHz watch crystal) and 2.4V supply. "Asleep" drain is 6 μA max. Extended-temperature-range devices (−40 to +85°C and −55 to +125°C) available, as well as extended-voltage-range devices.

COP400 FAMILY (NMOS MEMBERS)

PART NUMBER	MEMORY ROM (BYTES)	MEMORY RAM (DIGITS)	I/O PINS	INTERRUPT	STACK	TIMER BASE COUNTER	SIZE (PINS)	OTHER
COP410L	0.5k	32	19	NO	2 LEVEL	NO	24	
COP411L	0.5k	32	16	NO	2 LEVEL	NO	20	
COP413L	0.5k	32	16	NO	2 LEVEL	NO	20	PMP
COP414L	0.5k	32	16	NO	2 LEVEL	NO	20	PMP
COP420	1.0k	64	23	1 SOURCE	3 LEVEL	YES	28	MICROBUS
COP421	1.0k	64	20	NO	3 LEVEL	YES	24	
COP422	1.0k	64	16	NO	3 LEVEL	YES	20	
COP420L	1.0k	64	23	1 SOURCE	3 LEVEL	YES	28	PMP
COP421L	1.0k	64	20	NO	3 LEVEL	YES	24	PMP
COP422L	1.0k	64	16	NO	3 LEVEL	YES	20	PMP
COP440	2.0k	160	36	4 SOURCES	4 LEVEL	YES	40	MICROBUS
COP441	2.0k	160	23	4 SOURCES	4 LEVEL	YES	28	MICROBUS
COP442	2.0k	160	19	2 SOURCES	4 LEVEL	YES	24	
COP444L	2.0k	160	23	1 SOURCE	3 LEVEL	YES	28	
COP445L	2.0k	160	20	NO	3 LEVEL	YES	24	

NOTE: PMP IS POST-METAL PROGRAMMING.

HARDWARE — SUPPORT — SOFTWARE

Mole (microcomputer on-line emulator) consists of two hardware components and software for a host computer. The two hardware components are a general-purpose Brain board common to all National microcontroller μCs and a personality board specific to the particular National μC being supported (which plugs into the Brain board). COP is supported by one of the personality boards.
Application hot line: (408) 721-5582.

Mole software is intended for user's host computer and is written for MS-DOS and CP/M. Includes COP cross-assemblers.

COP800 — 8-BIT CMOS

AVAILABILITY: Now.
COST: $2 to $5 for standard parts in high volume.
SECOND SOURCE: Sierra Semiconductor.
CORE: Sierra is using COP800 core for custom designs for applications such as portable medical monitors and home security. According to National, the number of parts in the standard family is growing by more than 35% per year. National offers a configurable-controller approach based on a set of microcontroller building blocks.

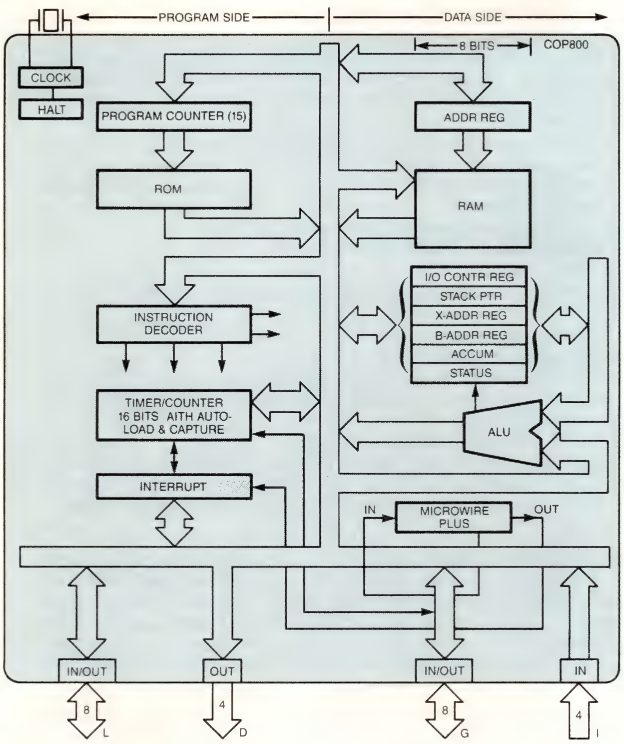
National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000

For more information, Circle No. 721

Description: 8-bit CMOS single-chip family in which a purposely simple core μP is surrounded by varying amounts of memory, peripheral functions, and I/O. Some 20 parts exist. Initial core has provision for addressing 32k-byte program memory and 256-byte data memory. The program and data memory are treated separately so, like the 4-bit COP400, the COP800 has a Harvard architecture. Otherwise, the COP800 seems more similar to Von Neumann common-memory machines such as Motorola's 6805 or National's 16-bit single-chip device, the HPC.

Status: Having gained one of the leadership positions in the 4-bit microcontroller field with its COP400 and having gotten 16-bit microcontrollers off to a start with its HPC16083, National introduced this 8-bit controller to fill the gap between those two devices. The architecture of the core μP seems quite simple—a bit like the Motorola 6508. National purposely kept the core simple and straightforward to leave room for lots of memory, peripheral functions, and I/O. Parts are built on National's double-metal process, shrinkable to submicron levels.

HARDWARE — CHARACTERISTICS — SOFTWARE



INDUSTRIAL VERSION (−40 TO +85°C)	MIL VERSION (−55 TO +125°C)	ROM/EPROM/ EEPROM (BYTES)	RAM (BYTES)	I/O PINS	INTERRUPT	TIMER BASE COUNTERS	SIZE (PINS)	OTHER
COP820C	COP620C	1.0k	64	24	3 SOURCES	1	28	
COP821C	COP621C	1.0k	64	20	3 SOURCES	1	24	
COP822C	COP622C	1.0k	64	16	3 SOURCES	1	20	
COP8640		2.0k	64	24	3 SOURCES	1	28	64 x 8-BIT
COP8641		2.0k	64	20	3 SOURCES	1	24	EEPROM
COP8642		2.0k	64	16	3 SOURCES	1	20	IN RAM
COP8620		1.0k	64	24	3 SOURCES	1	28	64 x 8-BIT
COP8621		1.0k	64	20	3 SOURCES	1	24	EEPROM
COP8622		1.0k	64	16	3 SOURCES	1	20	IN RAM
COP8720C		1.0k EEPROM	64	24	3 SOURCES	1	28	64 x 8-BIT EEPROM IN RAM
COP8721C		1.0k EEPROM	64	20	3 SOURCES	1	24	64 x 8-BIT EEPROM IN RAM
COP8722C		1.0k EEPROM	64	16	3 SOURCES	1	20	64 x 8-BIT EEPROM IN RAM
COP840C	COP640C							
COP841C	COP641C							
COP842C	COP642C	2.0k	128	24	3 SOURCES	1	28	
		2.0k	128	20	3 SOURCES	1	24	
		2.0k	128	16	3 SOURCES	1	20	
COP880C	COP680C	4.0k	128	36	3 SOURCES	1	40/44	
COP881C	COP681C	4.0k	128	24	3 SOURCES	1	28	
COP8780C*		4.0k EPROM	128	36	3 SOURCES	1	40/44	EPROM
COP8781C*		4.0k EPROM	128	24	3 SOURCES	1	28	& OTP
COP884CF	COP684CF	4.0k	128	21	10 SOURCES	2	28	2 PWM & A/D
COP884CG	COP684CG	4.0k	192	23	12 SOURCES	3	28	3 OWM & UART
COP884CL	COP684CL	4.0k	128	23	10 SOURCES	2	28	2 PWM
COP884CS*	COP6840CS	4.0k	192	23	12 SOURCES	1	28	1 PWM & UART
COP888CF	COP688CF	4.0k	128	33/37	10 SOURCES	2	40/44	2 OWM & A/D
COP888CG	COP688CG	4.0k	192	35/39	14 SOURCES	3	40/44	3 PWM & UART
COP888CL	COP688CL	4.0k	128	33/39	10 SOURCES	2	40/44	2 PWM
COP888CS*	COP6820CS	4.0k	192	35/39	14 SOURCES	1	40/44	1 PWM & UART

*AVAILABLE IN 1990
ALL DEVICES IMPLEMENT THEIR STACKS IN RAM AND HAVE AT LEAST 1 SERIAL I/O PORT

I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, and subtract with borrow.
Logicals include rotates, shift compares, and conditionals.
Decimal correct.
Increment and decrement.
Bit manipulation: set, reset, and test individual bits in data memory, which includes those in data registers and I/O ports.
II—DATA-MOVEMENT INSTRUCTIONS
Load and exchange instructions with optional automatic post increment or decrement of the associated pointer. Most allow the use of either the B or X pointer. Decrement register and skip if zero.
III—PROGRAM-MANIPULATION INSTR
Jump instructions: relative, absolute, absolute long, and indirect.
Subroutine, subroutine long, return, and skip (subroutine levels are limited only by the amount of available RAM).
Push and pop.
IV—PROGRAM-STATUS-MANIP INSTR
ALU-driven decision bits in status register (PSW) appear limited to carry and half-carry flags. These, as well as interrupt control bits for various on- and off-chip interrupt sources, can be set and reset.
V—POWER-SAVING INSTRUCTIONS
Halt mode, which is entered by setting data bit and exited by reset or low-to-high transition on the CKO pin.
Note:
1. Program-branch decisions are implemented in skip-the-next-instruction manner.

Specification summary: 8-bit Harvard (split-memory) architecture μC in CMOS. 15-bit program counter (PC) can address 32-byte program memory, which can include data and data tables. Initial on-chip memory selections are 1k, 2k, and 4k bytes. Selection of on-chip SRAM can be as large as 256 bytes. All data, control, and I/O registers are mapped into data-side memory space. Two bidirectional 8-bit and two unidirectional 4-bit I/O ports max. Each I/O pin has software-selectable options to adapt the chip to specific applications. Part may be operated in ROMless mode to provide for emulation and for applications requiring external program memory, in which case external memory is accessed serially via the I/O ports. On-chip peripheral functions include software-selectable I/O of as many as 39 I/O pins, 3-wire serial I/O, 16-bit timer/counter with capture register and auto reload, and an 8-source interrupt. Maximum speed is 1-μsec instruction cycle (most instructions take one cycle). Clock for 1-μsec cycle is 10 MHz. Operates over 2.5 to 6V range and draws 9 mA running full speed at 1-μsec cycles, but less than 1 μA when halted. Enclosed in 20-, 24-, 28-, 40-, and 44-pin DIPs and surface-mount packages. MIL-spec versions available.

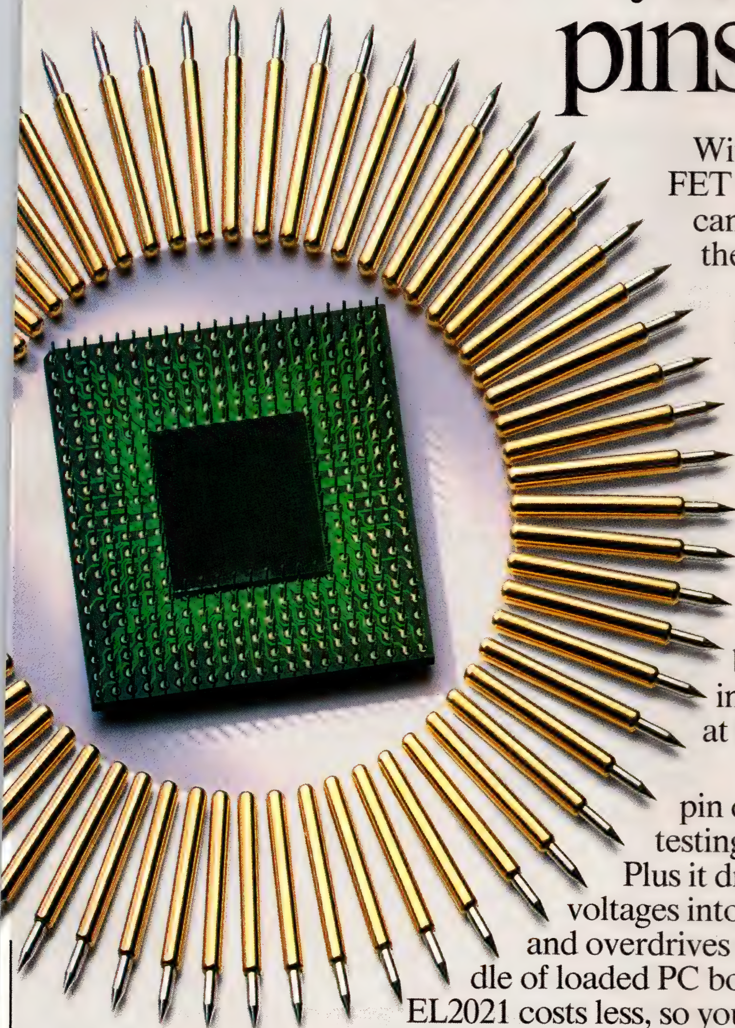
Hardware notes:
1. Diagram shows basic COP800-family architecture. Over 10 basic parts planned for the family. Each has an emulator part created by replacing standard masked-ROM with EEPROM.
2. The basic core, including CPU and some peripherals, is only 66 mils per side (4330 sq mils area), thus only taking up ⅒th of reasonable-sized chip (200 mils per side or 40,000 sq mils area) and leaving adequate room for not only basic memory and I/O but also for UARTs, A/D converters, additional timers, LCD display drivers, and custom features for specific applications. Sierra says cost of ASIC design can be as low as $40,000 up front (16 weeks' time), meaning ASICs can be cost competitive for 100k quantities.

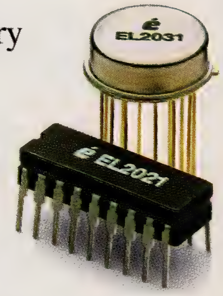
HARDWARE — SUPPORT — SOFTWARE

Supported on National COP800 Development Systems. The system can be used in conjunction with IBM PC as host.

Cross-assembler for IBM PC and other computers. Form-fit emulators are available for every member of the family. These parts are either piggybacks, 2-chip hybrids, or single-chip EPROMs or EEPROMs.

Thanks to Elantec, ATE design engineers are no longer kept waiting on pins and needles.





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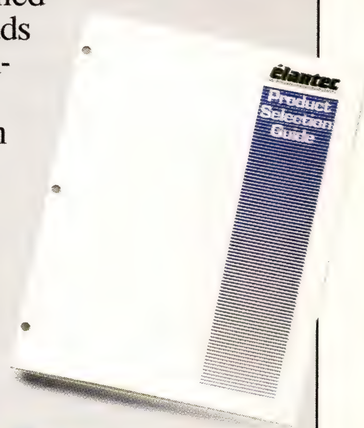

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8048 FAMILY

8-BIT NMOS AND CMOS

AVAILABILITY: Now.
COST: Masked-ROM parts less than $2 in high volume (100k). EPROM parts cost $18 (100). CMOS parts cost as little as $3 (100k). Windowless-PROM parts cost $8 (5000).
SECOND SOURCE: Toshiba, NEC, Signetics/Philips, National Semiconductor, Oki, Siemens, Fujitsu, GE-Intersil, UMC (Taiwan), with volume being spread out among suppliers.
CORE: Zymos has been using 80C49 as core for ASICs for a number of years. Others are following as 8048/49 combines widespread popularity with reasonably small core size.

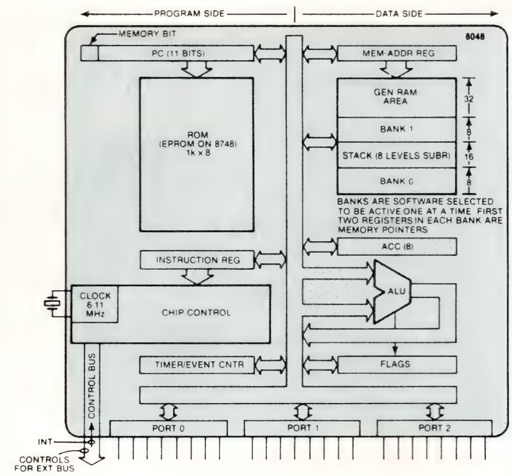
Description: Broad family of single-chip controller-type μCs, including version that can function as slave (8041). Basic models don't have serial communications ports (some versions from Philips do), but they can use 8080/85 peripherals for I/O expansion. See 8051 listing for enhanced version.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

For more information, Circle No. 722

Status: Intel is still bullish about the 8048. However, Intel chose the 8051 over the 8048 as the kick-off core for ASICs and says it has no definite plans to use the 8048 as an ASIC core.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram is for basic 8048. Table indicates some other basic parts, most of which exist in both NMOS and CMOS.
2. CMOS parts are designated 80C48, 80C49, 80C50, etc.
3. There are many other variations of the basic 8048 among the many suppliers. For example, Intel's 8041/42 chips are software compatible but can be configured as slaves to host μPs for interface applications. The National NS 405/455 uses the 8048 core as basis of a terminal controller. Siemens has telecommunications-oriented 80C382/482. A number of semicustom houses use the 8048 as a core processor in their libraries.

PART NO	MEMORY (BYTES)			PACKAGE PINS	
	ROM	EPROM	RAM	PARALLEL I/O	TOTAL
8035	0	0	64	3×8	40
8048	1k	0	64	3×8	40
8748	0	1k	64	3×8	40
8039	0	0	128	3×8	40*
8049	2k	0	128	3×8	40*
8749	0	2k	128	3×8	40*
8040	0	0	128	3×8	40
8050	4k	0	256	3×8	40

*ALSO AVAILABLE IN 44-LEAD PLCC PACKAGE.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Bit set and reset.
Two working banks of 8-bit registers.
II—DATA-MOVEMENT INSTRUCTIONS
Both internal and external RAM are fully accessible by instruction set.
Indirect and direct data fetches.
III—PROGRAM-MANIPULATION INSTR
Decrement and skip if zero.
Over 20 conditional branches.
8-level stack with expansion capability.
Two vectored interrupts.
Two programmable flag bits under software control.
IV—PROGRAM-STATUS-MANIP INSTR
Status word is fully accessible and is stored in the stack.

Specification summary: Split-memory architecture with 1k to 4k bytes of program ROM or EPROM on chip and 64 to 256 bytes in separate space, also on chip. I/O has its own space and instructions to operate directly on I/O ports. All spaces are expandable: program memory to 4k bytes, data memory to 256 bytes, I/O to unlimited amounts. I/O can use 8080/85 peripherals. Devices have 8-level stack for subroutine nesting and interrupt response. Dual banks of working registers allow rapid context switching. Family members execute their 1- and 2-cycle instructions at 1-cycle times ranging from 1.36 to 15 μsec. NMOS 5V technology in 40-pin DIP and 44-pad chip carriers; UV-erasable ROMs (EPROMs) and windowless PROM parts are available. CMOS versions available with idle and power-down features and optional flatpack packages.

HARDWARE — SUPPORT — SOFTWARE

From Intel: Intel plays down 8048 support, saying that there are now numerous third-party OEM suppliers of PC-hosted emulators for the 8048 family.
From NEC: Ekakit 84C-1 stand-alone emulator (less than $2000).

From Intel: ASM-48 package with linker to run on Intel microcomputer development systems running ISIS operating system ($1500 for 8-copy license).
From others: Because of the broad-based popularity of this family, dozens of independent sources of development and application software exist, including support on universal development systems from Tektronix and Applied Microsystems.
Program library: Insite Library contains variety of application programs.

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Inventors of the E^2CMOS PLD℠

Circle 55 for Literature
Circle 56 for Employment Information

8051/8052 FAMILY

8-BIT NMOS AND CMOS

AVAILABILITY: Now for 8051, 80C51, 8031, 80C31, 8751, 87C51, 80C32, 83C51FA, 87C51FA, 83C51FB, 87C51FB, 8032, and 8052.
COST: $2.70 (2k) for 8051; $33 (1k) for 8751; $3.30 (2k) for 80C51; $3.20 (2k) for 8052; $48 (1k) for 87C51; $42 (1k) for 8752; $5.30 (2k) for 80C52; $5.85 (2k) for 83C51FA; $57 (1k) for 87C51FA; and $65 (1k) for 87C51FB.
SECOND SOURCE: Siemens, Signetics/Philips, AMD, Fujitsu, Oki, and Harris-Matra (France) licensed.
CORE: Intel's ASIC Components Group is using the 8051 as its starting μP core.

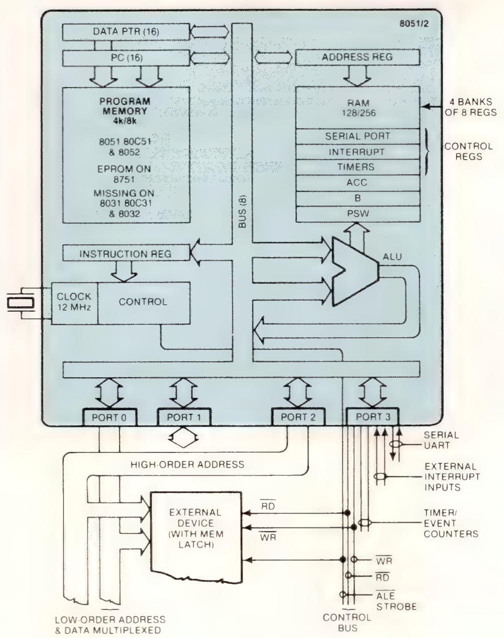
Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226

Phone (602) 961-8051 For more information, Circle No. 723

Status: Generally thought of as the leader among the newer, more powerful 8-bit single-chip μCs. This family faces stiff competition from high-end 8-bit μCs, such as Mitsubishi's 50740 version of the 6500/1, Motorola's 68HC11, NEC's 7811, Hitachi's 647180, and National's COP800, as well as from 16-bit μCs, such as Intel's own 8096 and National's 16040. The 8051 is among the most widely used cores in market-specific μCs.

Description: Expandable single-chip controller, an enhanced version of the same supplier's widely used 8048 family. Architecturally, it features the nonpaged form of addressing for easier programming; more interrupts with extra RAM register banks to service them; increased stack depth; and new instructions, such as multiply, divide, and compare. In peripheral support, the 8051 adds a full-duplex hardware UART and enlarged timer/counter capability.

HARDWARE — CHARACTERISTICS — SOFTWARE



Specification summary: Expandable single-chip μC. Split-memory architecture has 4k- to 8k-byte ROM on chip and 128 to 256 bytes of RAM on chip. Memories each expandable externally to 128k bytes. Four 8-bit ports on chip, but only one of these remains a port when all off-chip expansions and on-chip special functions are used. Special functions included on chip are full-duplex hardware UART (to 500k baud), two or three 16-bit timer/counters, and interrupt system to service these internal functions along with two external interrupts with 3-to 7-μsec latency. Instructions are a superset of the 8048s, with paged addressing eliminated. At 12-MHz clock frequency, most instructions take 1 μsec; multiply or divide requires 4 μsec. Supplier's high-density HMOS silicon-gate n-channel technology used to achieve small die size and speed. Packaged in 40-pin DIP and 44-pad chip carriers. 8051 is also available in CMOS (80C51) with 12- or 16-MHz performance and idle/power-down modes.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including add, subtract, multiply, and divide.
Bit manipulation, including complex tests on bits and branching on results.
II—DATA-MOVEMENT INSTRUCTIONS
Register addressing for the eight working registers in the four register banks.
Direct, immediate, and indirect data addressing for more general data accessing.
Table look-up in ROM via data pointer.
III—PROGRAM-MANIPULATION INSTR
Depth of subroutining limited only by available space in 128- or 256-byte on-chip RAM.
Conditional jumps on status-register flags.
Conditional jumps on comparisons.
Vectored interrupts to service two external interrupts, timers, and UART.
IV—PROGRAM-STATUS-MANIP INSTR
CPU's program-status word fully accessible via software. Status bits in timer and UART also software accessible.

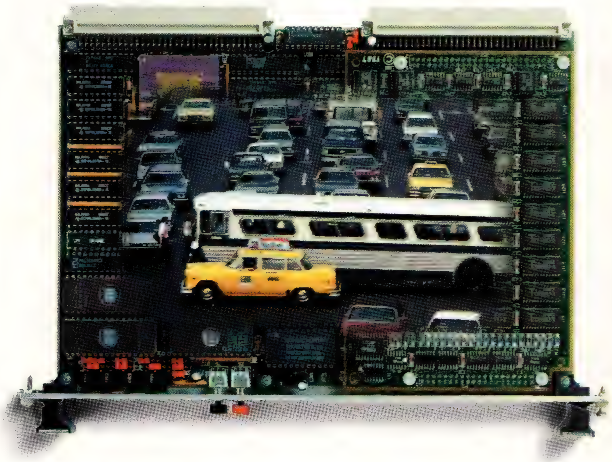
Notes:
1. The 14 members of the 8051 family have between 128 and 256 bytes of RAM and differ mainly in their amount and form of on-chip ROM. The 8051 and 80C51 incorporate 4k bytes of masked ROM. The 8751 and 87C51 have 4k bytes of EPROM. The 83C51FA has 8k bytes of masked ROM and a programmable counter array (PCA). The 87C51FA has 8k bytes of EPROM and a PCA. The 8031, 80C31, and 80C51FA have no on-chip ROM. Hence, because they must use ports to access external memory, only port 1 is available for I/O. The 83C51FB and 87C51FB are 16k-byte-memory versions of the FA versions. The 8052 and 80C52 have 8k bytes of masked ROM. The 8032 and 80C32 have no on-chip ROM. The 8052, 8032, 80C52, and 80C32 have 256 bytes of on-chip RAM.
2. The 8051's Boolean-processor capabilities refer to the way instructions can single out bits in RAM, accumulators, I/O registers; perform complex bit tests and comparisons; then execute relative jumps based on results.
3. The slave version of the 80C51, the UPI-452, is counterpart of UPI-42 (8041/42) for the 8048 family. It is intended for software-customizable interfaces.
4. Intel has one model of 8052 preprogrammed with a full Basic interpreter.

HARDWARE — SUPPORT — SOFTWARE

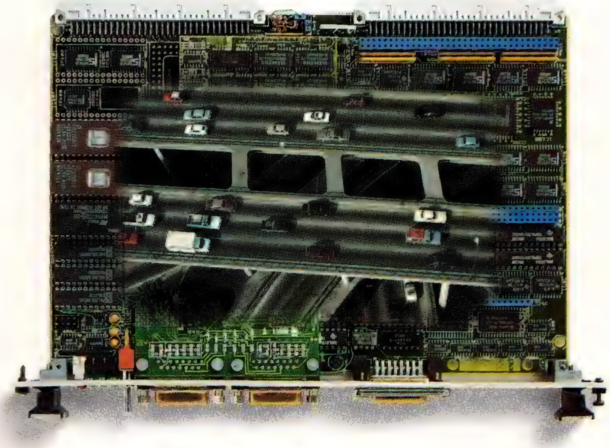
From Intel: ICE-5100/252 in-circuit emulator ($5495) supports the entire MCS-51 family including 8051, 8052, and 80C52. Comes with macroassembler and editor. The emulator is hosted on an IBM PC AT/XT running DOS 3.1 or later versions, as well as on Intellec Series III/IV development systems.

From Intel: ASM-51 and PL/M-51, both containing a relocation and linkage utility, are available for the IBM PC and Intel microcomputer development systems.
From others: A number of third-party software suppliers have developed C compilers for 8051 that have special features suited to microcontroller applications. Two such compilers are Micro Computer Control's (Hopewell, NJ) for $1495 and Archimedes Software's (San Francisco, CA) for $851. Both are hosted on IBM PC.

THEMIS SINGLE BOARD COMPUTER ELIMINATES DATA-FLOW BOTTLENECKS



Arbitration Delays



Concurrent Transfers

Until now shared memory architectures have resulted in data-flow bottlenecks. The resulting arbitration delays cause unpredictable data transfer latencies, unwelcome in real-time systems.

The Themis TSVME 133 relieves this shared resource bottleneck by providing dedicated paths and memories for high speed transactions. Thus, three levels of concurrent operation are possible:

- 68030 Transfers with Local Memory
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If you have to manage VMEbus, VSB, Ethernet, SCSI, FDC and Serial-line ports, the TSVME 133 will keep your data moving!

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CIRCLE NO 57

6804/6805

8-BIT NMOS AND CMOS

AVAILABILITY: Now for most models.
COST: $1 to $8. CMOS parts are more expensive than NMOS ones.
SECOND SOURCE: Harris, Hitachi, and SGS Thomson.
CORE: Motorola and NCR have joint ASIC pact to use CMOS 6805 as core along with NCR's similar 6502 μP core. SGS Thomson has ST6 core, which has architecture somewhat similar to 6804's.

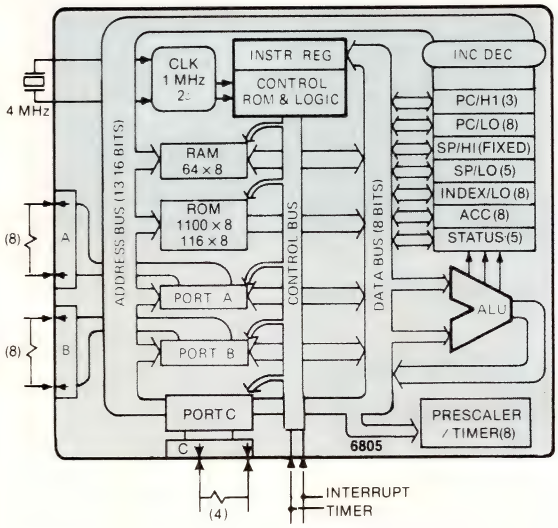
Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 440-2000

For more information, Circle No. 724

Description: Family of single-chip μCs based loosely on 6800 architecture but in some ways more like 6502 (especially 6805). Family offers various amounts of I/O, RAM, and ROM. Internal bus frequencies span dc to 4 MHz. Some parts contain an on-chip A/D converter, EEPROM, serial I/O, and software security. 6804s are meant for lowest-end applications. They use some serial data paths internally to reduce chip size.

Status: Supplier's steady commitment to this family over past 11 years has paid off. It trails only the 8048/49 family and the 50740 in market share. Motorola continues to expand the 6805 family.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram is for nonexpandable Model P2 in 28-pin package.
2. Comparison of 6805 with 6800: Stack pointer has only five working bits, so stack is only 32 bytes deep. Only one accumulator. Index register only 8 bits wide, so it can only span 256 memory locations. However, a 16-bit offset addressing mode is supported on all members of this family, thus 256-byte tables can be accessed anywhere within the memory space. Program counter only 11 bits, which is adequate for P2's 2k-byte RAM + ROM memory space; the program counter is as long as 14 bits in some members of this family. Only one external interrupt is provided, but some models have timer-input capture pins, which may provide additional edge-triggered inputs.
3. Note additional 116 bytes in ROM for built-in self-check program that tests I/O, ROM pattern, RAM, and interrupts. Program is initiated by special pin.
4. Harris has emulator versions (68EM05/C4,D2) for prototyping and low-volume production. These are ROMless devices with all ROM access buses brought out for direct interfacing to industry-standard EPROMs. Available in 40-pin piggyback for 2764.

I—DATA-MANIPULATION INSTRUCTIONS
All 6800 arithmetic, logic, and shift instructions. Bit set, clear, and branch on bit test. Bit tests can be made on all I/O and memory bits. 68HC05 has 8 × 8-bit multiply.
II—DATA-MOVEMENT INSTRUCTIONS
Relative addressing allows data relocation.
True indexing within the 256-location limits of 8-bit index.
III—PROGRAM-MANIPULATION INSTRUCTIONS
18 conditional branches, including branch of interrupt line test.
Mostly the same conditional branches as the 6800, but with more emphasis on branch-upon-bit and interrupt tests.
Only 15 levels of subroutine nesting, including interrupt returns; 31 levels on certain new parts.
Four sources of interrupts: external, timer, software, and reset. 68HC05 has vectored interrupts to service its serial-communications and peripheral interfaces
IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Instructions for manipulating bits in status register and timer.
V—POWER-SAVING INSTRUCTIONS
CMOS 6804s and 6805s have Stop and Wait instructions and will safely reset themselves when the clock is reapplied.

Specification summary: Common-memory architecture in which instructions, data, I/O, and timers all share the same memory space. This scheme allows I/O to be bit rotated and bit manipulated. Dedicated bit manipulation includes bit set/clear and branch on bit set/clear. A 4-MHz oscillator provides a 1-MHz internal cycle on most 6805 versions. New 68HC05s have a 2.1-MHz internal bus speed. Some, like the 68HC705C8, available with a 4-MHz bus speed. Included are parts with program security, on-chip EEROM, A/D converter, serial peripheral interface, serial communications interface, and PLL frequency synthesizer. Family consists of NMOS and CMOS parts in 20-, 28-, and 40-pin DIPs and chip carriers. NMOS requires 5V supply; CMOS operates over 3 to 6V.

FAMILY		SPEED BUS (MHz)	INSTRUC-TIONS	ON-CHIP ROM	RAM	I/O PINS	TIMER	INTER-RUPTS	POWER CONSUMP-TION (mW)	PINS
6804	MIN	0	42	0.5k	32	16	—	3	0.01	20
	MAX	2	42	2k	128	20	YES	4	~400	28
6805	MIN	0	51	1k	64	16	—	3	0.01	28
	MAX	2	59	4k	176	32	YES	5	~700	40
68HC05	MIN	0	62	2k	96	32	YES	2	0.25	40
	MAX	4	62	7.7k	176	32	YES	2	0.25	40

HARDWARE — SUPPORT — SOFTWARE

From Motorola: HDS-200 hardware/software development station, operates independently or interfaced to virtually any host with an RS-232C line, including Motorola's Exor stations. The less-costly 68705EVM (HMOS) and 1468705EVM (CMOS) boards, which have ports to a terminal and host computer, provide target-system emulation.
From RCA: Single-board evaluation kit that interfaces to IBM PC via RS-232C line.
From others: A number of third-party companies provide hardware emulators for the 6805 family, including Sophia Systems (Santa Clara, CA) and American Automation (Tustin, CA). Most of these emulators interface to IBM PCs.

From Motorola: Software can be obtained free for downloading over phone lines by calling (512) 440-3733.
From others: Many cross macroassemblers and linking loaders, some relocatable. RELMS (San Jose, CA) has cross support for Intel development systems. Avocet Systems Inc (Rockport, ME) has cross-assemblers for 6805 and 6804 that run on IBM PC and compatibles. Introl (Milwaukee, WI) provides cross-compilers and cross-assemblers.

Text continued on pg 116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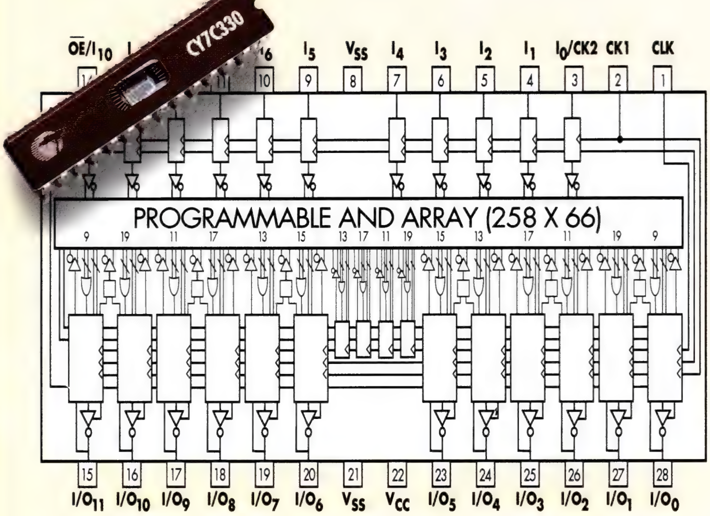
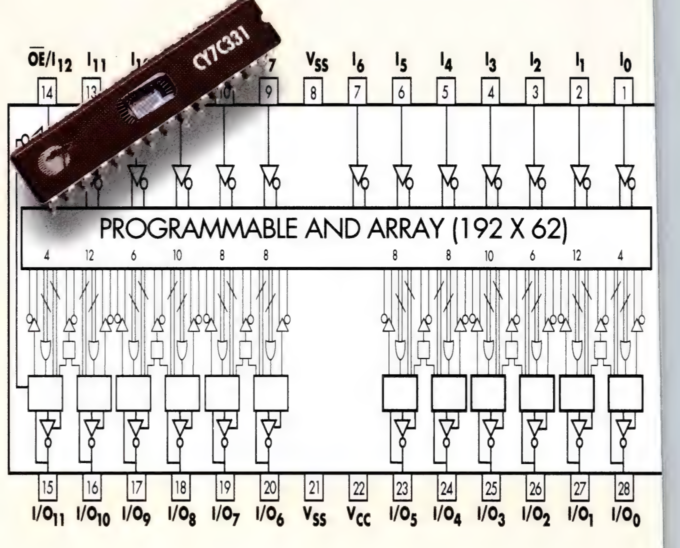
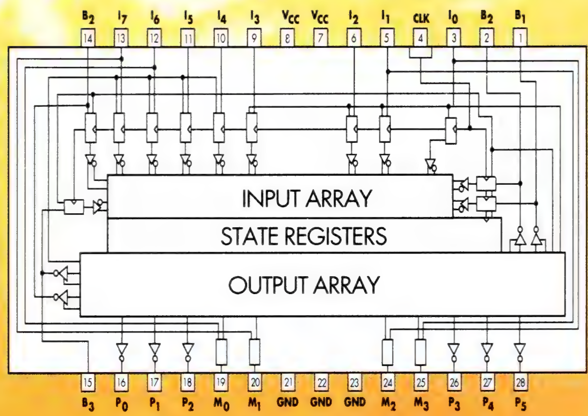


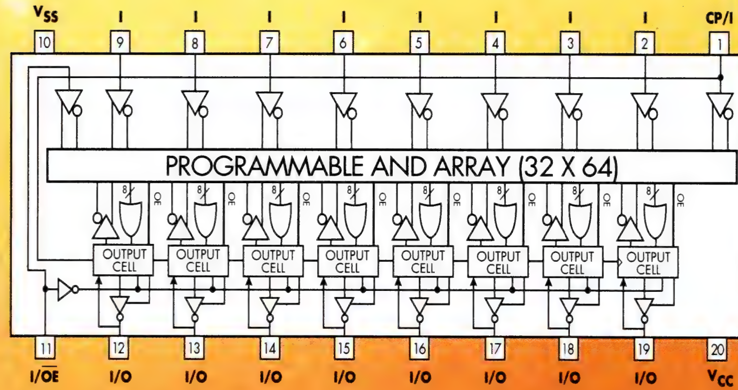
CY7C330
66 MHz Synchronous State Machine PLD



CY7C331
20ns Asynchronous Registered PLD

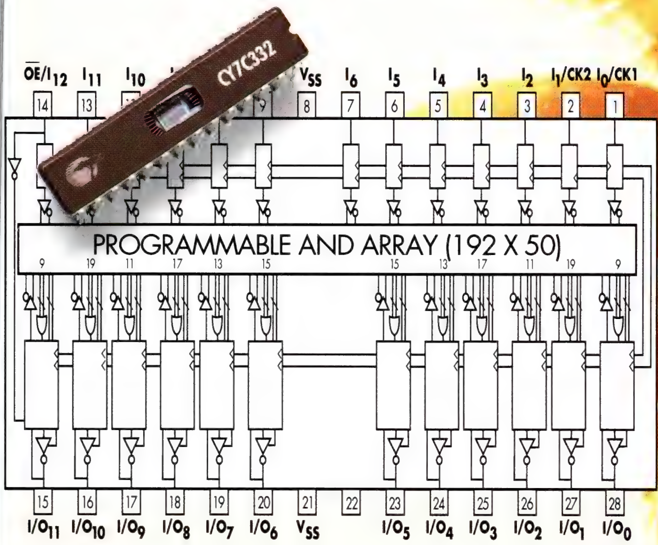
Replace up to 12 TTL parts, at





CY7C361
125 MHz Ultra High Speed
State Machine EPLD

CY10E301
2.5ns ECL PLD



CY7C332
15ns Input Registered Combinatorial PLD

Reprogrammable Ultra High Performance PLD.

speeds to 125MHz.

CY7C330 Synchronous State Machine PLD. 66MHz.

Fast enough to run at 66MHz without breathing hard. Created for state-machine sequential logic, so it is easy to program, and delivers very efficient state-machine functionality. With 258 product terms, you have the flexibility you need to create high performance logic quickly and elegantly.

CY7C331 Asynchronous Registered PLD. 20ns.

The only PLD that can *self-time* asynchronous, sequential operations.

You get product term control of set, reset, and clock. You get the flexibility of 192 product terms and multiplexed I/O Macrocells. And you get speed. 20ns maximum input to output.

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The high performance solution for combinatorial applications. You get twice the logic capacity of previous-generation combinatorial PLDs, and 50% more speed than any CMOS PLD with comparable logic capability.

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Logic to keep pace with the truly high-revving microprocessors. Cache and I/O subsystem control, numeric processor control, asynchronous dataflow applications, to name a few, are simplified and accelerated with this high performance PLD.

CY10E/100E301 and CY10E/100E302. ECL PLD. 2.5ns.

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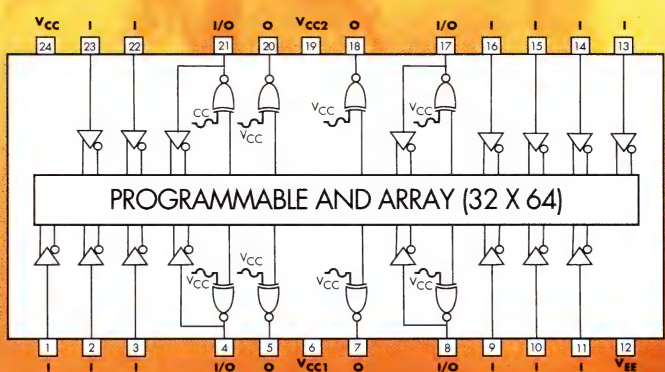
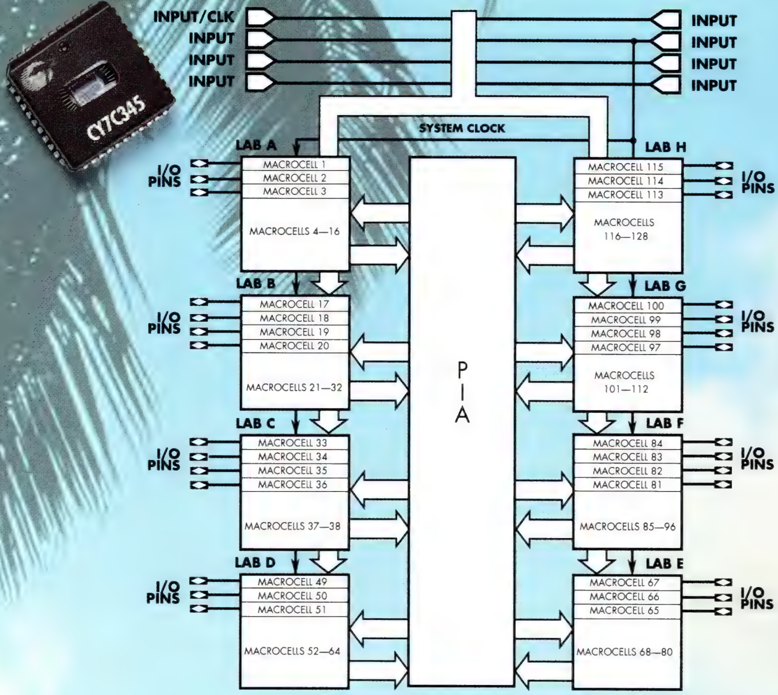
PLD C 18G8 Universal 20-pin Programmable Logic Device. 12ns.

Here is our newest reprogrammable CMOS PLD — a universal device that replaces a huge range of logic functions, from 10H8 and 18P8, to 16V8 and 18U8 with just about every configuration in between. Simpler inventory. Much faster part.

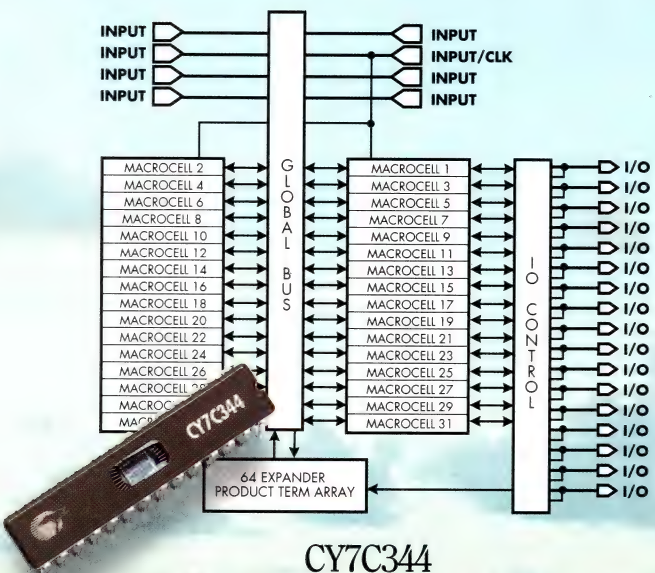


PLD C 18G8
12ns Universal 20-pin Programmable Logic Device

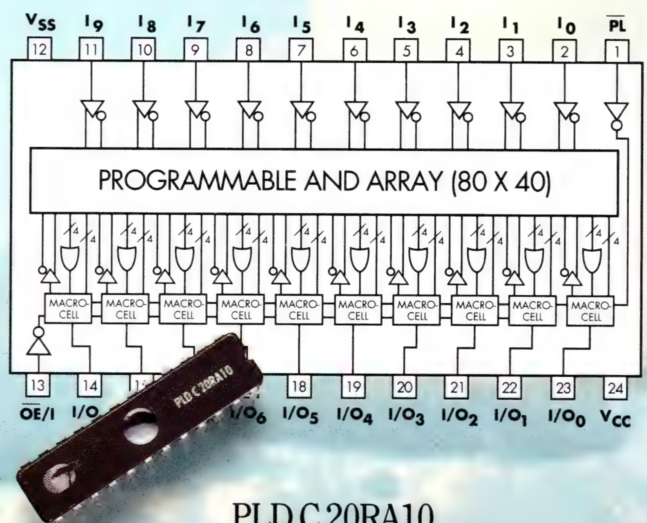


CY7C345
30ns 128 Macrocell MAX PLD

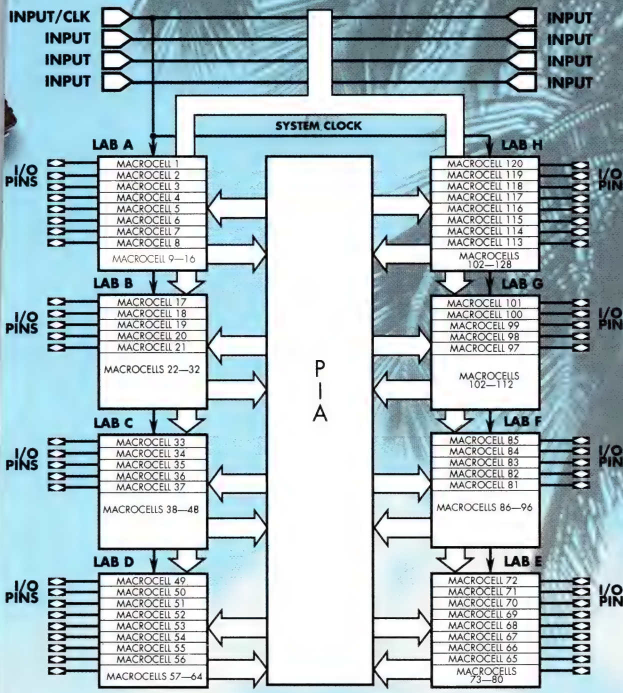
Replace up to 50 TTL parts, a



CY7C344
20ns 32 Macrocell MAX PLD

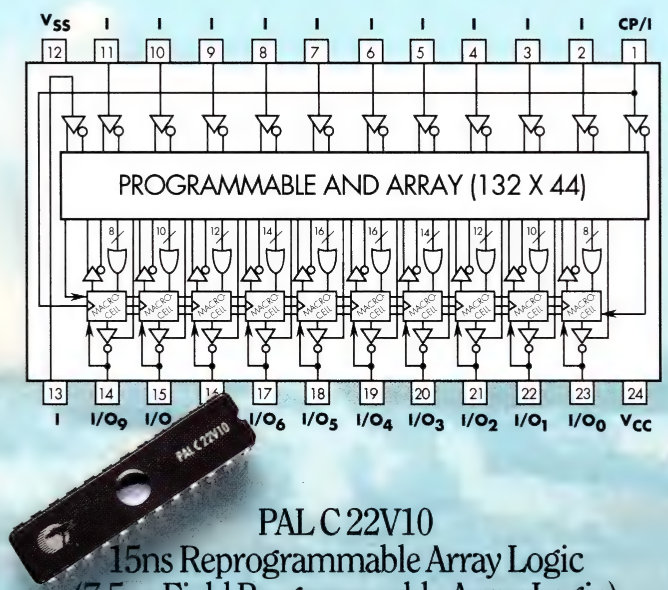


PLD C 20RA10
20ns Asynchronous PLD



CY7C342
30ns 128 Macrocell MAX PLD

speeds to 50MHz.



PAL C 22V10
15ns Reprogrammable Array Logic
(7.5ns Field Programmable Array Logic)

Reprogrammable High Performance PLD.

CY7C340 Multiple Array Matrix (MAX™) PLD Family. To 50MHz.

This family extends the benefits of Programmable Logic to logic densities that once required gate arrays, up to 50 separate TTL parts, or up to 15 PLDs.

Compared to using multiple TTL devices, you save board space, power, cost, and design time.

Compared to using small gate arrays, you save NRE, design time and gain considerable control through reprogrammable bench-level development.

50MHz speed, with high density.

The architecture of Macrocells grouped into Logic Array blocks gives you tremendous design flexibility.

The architecture is optimized for variable product terms. The grouping of Macrocells into Logic Array Blocks offers additional flexibility through Expander Product Terms which can be shared between Macrocells.

This means you can implement as many as 35 product terms in a single Macrocell.

	7C344	7C343	7C345	7C342
Macrocells	32	64	128	128
MAX FlipFlops	32	64	128	128
MAX Latches	64	128	256	256
MAX Inputs	24	36	36	60
MAX Outputs	16	28	28	52

PLD C 20RA10 Programmable Logic Device. 20ns.

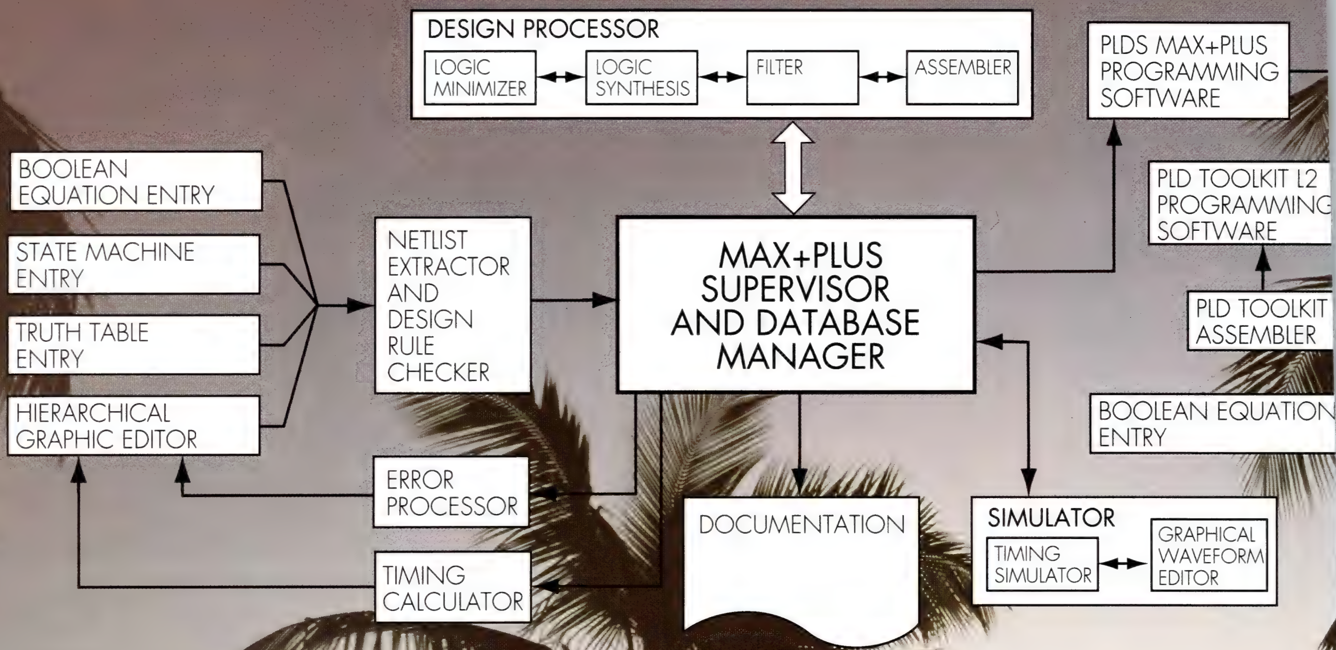
Here is an improved, low power version of this popular, high-performance part. You get an extremely fast, cost effective solution for asynchronous logic designs in the 200-400 gate range.

PAL C 22V10 Programmable Logic Array. 15ns.

Programmable Macrocells deliver the flexibility to implement product terms sufficient to replace logic in the 500 gate complexity range.

Our high performance 0.8 micron CMOS process gives you the flexibility of reprogrammability, very small package sizes, low power draw, and speed, speed, speed.

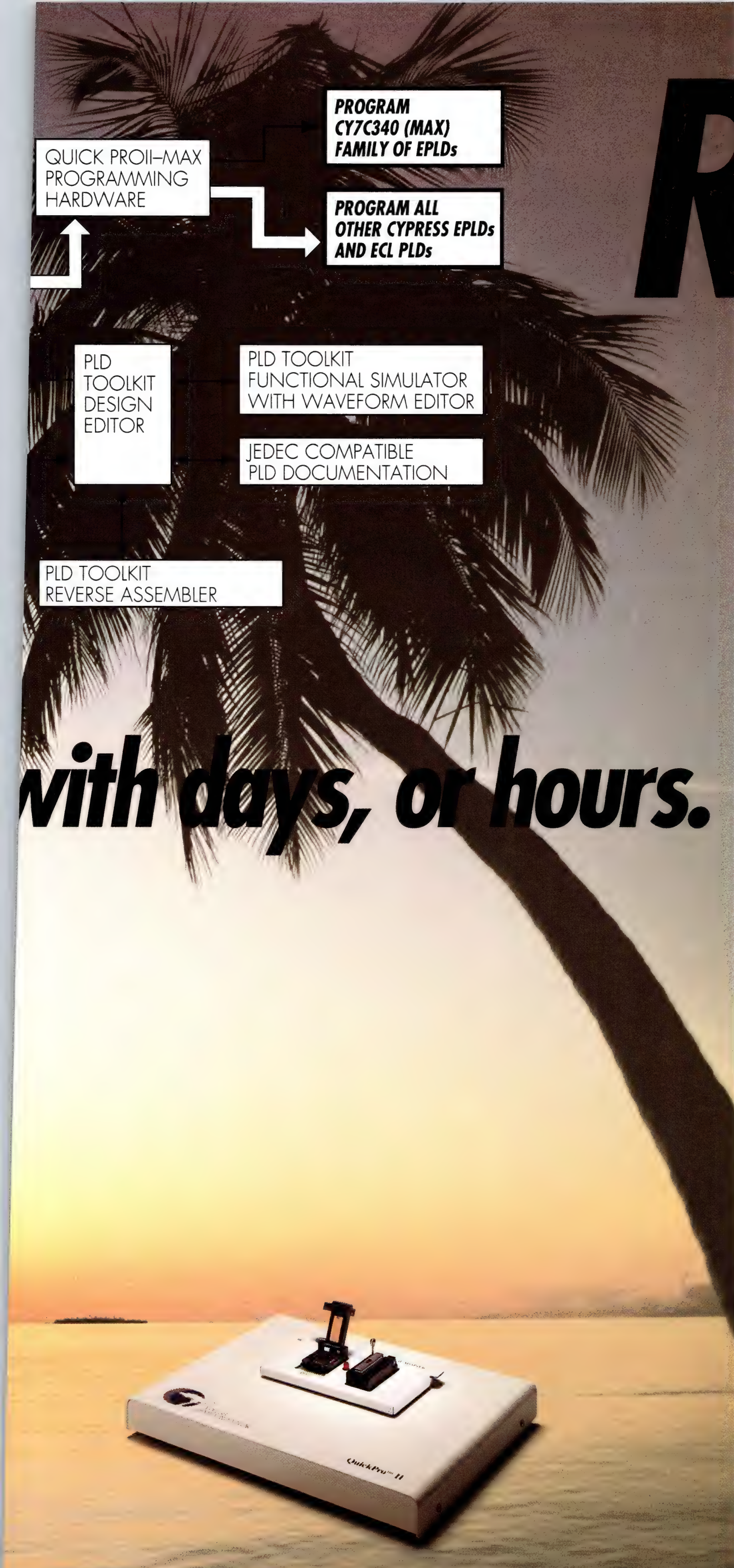
A best-seller for good reasons.



Replace weeks of logic design

MAX+Plus ToolKit.

PLD ToolKit.



QuickPro II Programmer

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Our force of talented, helpful Field Application Engineers.

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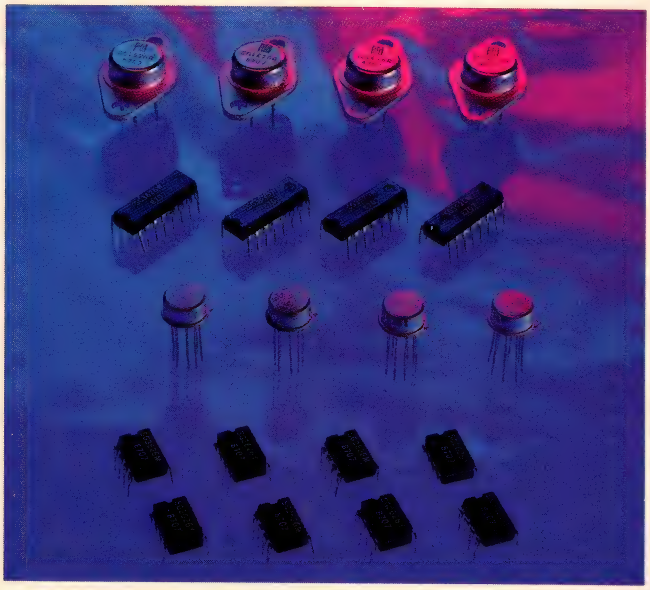

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The SG1626 is pin for pin compatible with National's DS0026, Motorola's MMH0026, Teledyne's TSC426 and Intersil's ICL7667.

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To arrange shipment of sample quantities and/or receive full technical information, please address Silicon General, Inc., Semiconductor Group, 11861 Western Avenue, Garden Grove, California 92641. Telephone (714) 898-8121. TWX: 910-596-1804. FAX (714) 893-2570.

SILICON GENERAL

6801/6301/68HC11 — 8-BIT NMOS AND CMOS

AVAILABILITY: Now.
COST: From less than $3 to $20 (1k).
SECOND SOURCE: SGS Thomson and Toshiba. Toshiba is a second source for the 68HC11 devices.

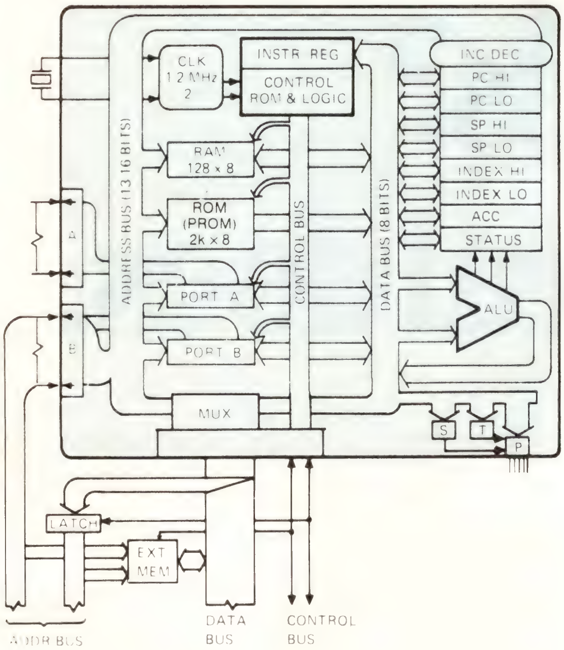
Description: 6801 is large, expandable, single-chip version of the 6800, with enhancements that include 10 more instructions, serial I/O, 8×8-bit multiplication, and a multifunction 16-bit timer. 6301 is slightly enhanced CMOS version; 68HC11 is further enhanced in static CMOS. 68HC11 has a second 16-bit-wide register; an 8-function timer; a 2-function pulse accumulator; an enhanced UART (SCI); a 1-MHz serial shifter; an 8-channel, 8-bit A/D converter; and a 512-byte EEPROM.

Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 440-2000

For more information, Circle No. 725

Status: This family has been well received. Motorola is now following migration of customers to more powerful single-chip devices and is concentrating on the 68HC11 enhancement of the 6801, such as increased on-chip EEPROM. During early 1990, Motorola will offer the 68HC711D3 with 4k bytes of EPROM in a one-time programmable package.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Instructions to take advantage of two accumulators, including 8×8-bit multiply. 68HC11 has additional 16-bit operations, integer and fractional divides, and bit manipulation.
II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions.
Can list-process efficiently with the index register (two on 68HC11) and can add accumulator to index register within a 64k-byte range.
Relative addressing allows data relocation.
Has 16-bit load and store.
III—PROGRAM-MANIPULATION INSTRUCTIONS
Has PDP-11 branches and conditional branches. Has unlimited subroutine nesting via stack pointer, addressing LIFO stacks in RAM.
Eight levels of prioritized, vectored interrupts (21 on 68HC11).
IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Instructions for storing status register or transferring to or from accumulator. 68HC11 has additional active bits related to stop mode.
V—POWER-SAVING INSTRUCTIONS
6301 has sleep instruction. 68HC11 has Stop and Wait instructions similar to 146805 but with disabling provision via a bit in status register.

Hardware notes:
1. Diagram is for 6801. See table for other family members.
2. Motorola is providing OTP versions of some HC11 family members, which have EPROM program memories in inexpensive windowless packages for one-time programming in moderate-volume production (to 10k).
3. Motorola's 68HC11 is a much enhanced 6801. 68HC11A8 has a 512-byte EEPROM; 68HC811E2 has a 2k-byte EEPROM.

Software notes:
1. 6801 has all 6800 µP instructions plus 10 new ones to handle additional resources such as advanced serial I/O ports and timers.
2. 68HC11 has enhanced 6801 instruction set with 88 additional op codes.

PART	DESCRIPTION	MEMORY ON CHIP ROM	MEMORY ON CHIP RAM	MEMORY EXT	INTERNAL BUS SPEED	I/O PAR	I/O SER	TIMER EVENT CTR	EXT INTS	PINS
6801	EXPANDABLE 1-CHIP µC	2k	128	64k	0.5M–2.0M	29	3	3×16	2	40
68701	EPROM VERSION OF 6801	2k	128	64k	0.5M–2.0M	29	3	3×16	2	40
6803	ROMLESS 6801	—	128	64k	0.5M–2.0M	13	3	3×16	2	40
68HC11	CMOS WITH UART, SPI, SERIAL, 8-BIT A/D	8k (ALSO 512 EEPROM)	256	64k	0–2.1M	28 32	6	4×16	2	48 (DIP) 52 (QUAD)

Specification summary: Expandable single-chip µC with common-memory architecture in which all instructions, data, I/O, control, and data registers share the same memory space. This scheme allows I/O to be handled like memory with all instructions applying. Instruction set is upwardly compatible with 6800, with 10 additional instructions for 6801 and 88 new op codes for 68HC11. The ROM, RAM, and I/O resources for 6801 and 68HC11 families are detailed in table. Internal bus speed to 2 MHz for 6801 and from dc (asleep) to 2.1 MHz for 68HC11. The 6801 is fabricated in NMOS, the 6301 is fabricated in CMOS, and the Motorola 68HC11 is fabricated in static CMOS to allow dormant, micropower "asleep" state. 6801 in 40-pin DIP, 6301 in 64-pin DIP and flatpack, and 68HC11 in 48-pin DIP and 52-pin quad.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: Software can be obtained free for downloading over phone lines by calling (512) 440-3733. C compiler to run on Unix System V for 68HC11. For least expensive approach, use 6801 parts with LILbug monitor in on-chip ROM (MC6801L1).
From others: Cross macroassemblers and linking loaders, some relocatable, to run on popular minis and personal computers. For example, C compiler from Archimedes (San Francisco, CA) to run on IBM PC ($995) and DEC VAX ($3995 to $5995).

From Motorola: For 6801 family, M68701EVM is evaluation module that has port for terminal and port for any RS-232C host and will program 68701 EPROM parts. For 68HC11, the similar M68HC11EVM. Also M68HC11EVB boards ($168.11) for evaluating single-chip configuration of HC11s. For both 6801 and 68HC11, HDS-300 software-development station operates independently or interfaced to most any host with RS-232C port.
From others: Third-party hardware development systems, such as CT68HC11 ($5000 to $6000) from Ashling Microsystems Ltd (Limerick, Ireland).

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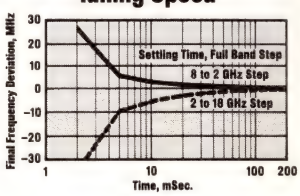

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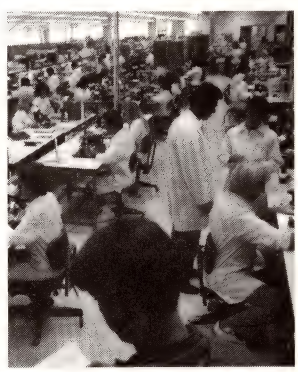


AVANTEK

CIRCLE NO 73

6500/1, 65C124, 50740, 37700

8-BIT (AND 16-BIT) NMOS AND CMOS

AVAILABILITY: Now for all NMOS and most 8-bit CMOS parts.
COST: Prices range from $2 to $20 according to complexity of part and volume. Volume-leader Mitsubushi's prices range from $3 to $30.
SECOND SOURCE: NCR (licensed) and California Micro Devices for Rockwell NMOS parts. Western Design Center (WDC) has licensed a number of suppliers worldwide for its CMOS designs.
CORE: Standard megacell in libraries of NCR, Mitsubishi, WDC, SMC, and several others. Widely used because of compact 6502 die size.

Description: There are three different sources for single-chip versions of 6502 µP: the original 6500/1 NMOS family from Rockwell, the new 65C124 and -134 CMOS family from WDC, and the 50740 CMOS family from Mitsubishi. Most parts are 100% software compatible with 6502, although in some cases enhanced instructions such as bit manipulation have been added. Because of small die size of 6502 core, many of these parts take a standard-cell ASIC approach. Vendors claim these 1-chip sets have a speed advantage over competing single-chip devices due to 6502's 2-cycle bus and pipelining.

Status: Mitsubishi's 50740 Series is a top volume leader among 8-bit µCs, along with the 8048/49, 6805/6801, and 8051 µC families. Mitsubishi's explanation for the part's market share is that the 50740 is used in Japanese consumer products. According to Mitsubishi, you will find standard or custom 50740s if you open products from Hitachi, JVC, Sanyo, or Minolta.

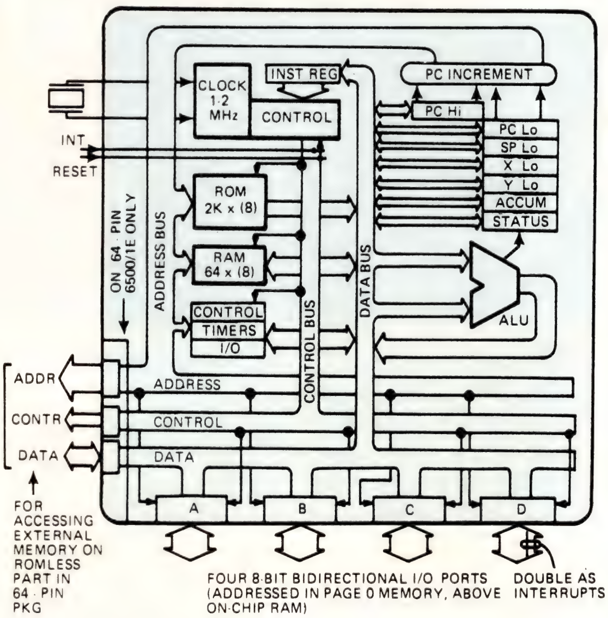
Rockwell International
Semiconductor Products Div
4311 Jamboree Rd
Newport Beach, CA 92658
Phone (714) 833-4600

For more information, Circle No. 726
Mitsubishi Electronics America Inc
1050 E Arques Ave
Sunnyvale, CA 94086
Phone (408) 730-5900

For more information, Circle No. 727
Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
Phone (602) 962-4545

For more information, Circle No. 728

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram favors initial Rockwell 6500/1 version. There are dozens of versions from various sources, most of which are more complex.
2. Mitsubishi 740 Series parts are all CMOS and have as many as 16k bytes of ROM and 512 bytes of RAM. Some models have special functions such as UARTs, 8-bit A/D converters, LCD drivers, or high-voltage (−35V) outputs. Some have 56 pins of I/O.
3. Mitsubishi's new CMOS M37700 version has an 8-bit external data bus but will be 16 bits internally, much like the 68C816 version of the 6502 µP. On chip it can have as many as 32k bytes of ROM, 2k bytes of RAM, eight 16-bit timers, two UARTs, one watchdog timer, and an 8-channel 8-bit ADC. It is expandable to 16M bytes off chip.
4. WDC's first part, 65C124, has been joined by 65C134—a 6502 core µP—which includes a LAN connection.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logical. Decimal mode via control bit in status register. Can operate on locations in memory space, which can be either RAM or I/O ports.
Bit-manipulation enhancement on some models allows bit set and reset and branching on bit set or reset.
II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, though index offset limited to eight bits in two CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables.
III—PROGRAM-MANIPULATION INSTRUCTIONS
Conditional branches with signed relative addresses.
Nonmaskable and/or maskable interrupt, depending on model.
IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Push and pull status register from memory stack. Set and clear carry, decimal mode, and interrupt bits.

Software notes:
1. 6500/1 instruction set is 100% identical to that of previous 650X family devices such as 6502, with exception of bit-manipulation instructions for some devices. No new instructions added to handle new on-chip features such as timers and I/O because they are handled as if in external memory space.
2. Mitsubishi chips have some added instructions.

Specification summary: Single-chip nonexpandable and expandable versions of 650X family. Have 2k- to 16k-byte ROM, 64- to 512-byte RAM, as many as 52 I/O lines, and one or more 16-bit programmable interval timers, as well as two or more programmable interrupts (plus the 650X's NMI interrupt). Family options (Rockwell) include RS-232C port and bus expansion. Operates from 5V, 500 mW, and has separate 5V supply to keep 64 static bytes of RAM alive (50 mW required). Wide variety of package types and sizes from various suppliers ranging to 80-pin flatpack and 84-pin PLCC from Mitsubishi. Full MIL-SPEC temperature-range devices from WDC.

HARDWARE — SUPPORT — SOFTWARE

From Rockwell: Emulator part, the 64-pin 6500/1E ($75), is used in R6500/1 personality card ($995), which plugs into LCE System ($1250). Backpack part will be ROMless 40-pin R6500/1EAB ($42), into which industry-standard EPROMs can be plugged.
From Mitsubishi: Debugging machine PC4000E ($1000) with in-circuit-emulator (ICE) cards for each device model ($750 to $1500).
From WDC: Toolbox Design System ICE for W65C124 runs on an Apple IIGS host and can communicate with an IBM PC via a serial port ($4995).

From Rockwell: Because the 6500/1 emulator runs on LCE system and Aim-65 (Dynatem, Irvine, CA), you can use existing 6502 program-development software. A debug monitor is available for all 6500/1 and 6500/11 devices, and the macroassembler supports enhancement instructions. Cross software available.
From Mitsubishi: Cross software for MS-DOS. (Has plans for a C compiler and Forth interpreter.)
From WDC: Many software packages available from third parties for the W65C02/W65C816 µPs.

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NS Bldg 8F
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Tokyo 163 Japan

CIRCLE NO 60

Z8, SUPER8

8-BIT NMOS AND CMOS

AVAILABILITY: Now for 2k-byte, 4k-byte, and ROMless parts at 8 to 12 MHz and Super8. Sharp and Zilog have CMOS now. SGS Thomson has 4k-byte EPROM and 8k-byte ROM.
COST: Less than $3.50 for NMOS Z8 in volume. $3.60 for NMOS Super8 in volume. (28-pin version for $1.) Less than $5 for CMOS Z8.
SECOND SOURCE: SGS Thomson (licensed); Sharp for both NMOS and CMOS; Catalyst for EPROM version; VLSI Technology for CMOS.
CORE: From Zilog and VLSI Technology. SGS Thomson's ST9 core is based on Super8 architecture.

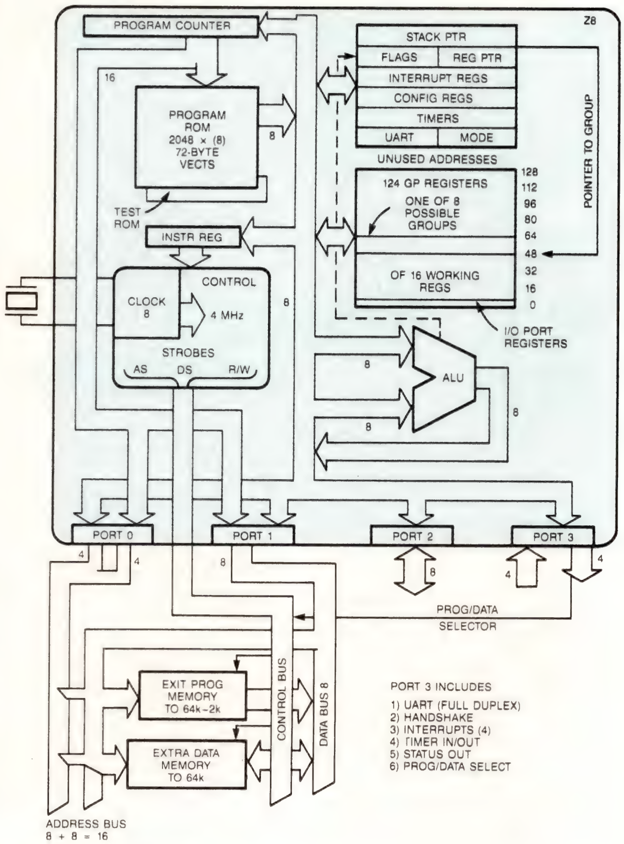
Description: Z8 is a single-chip μC that is a composite of many machines. It has powerful features that can't necessarily be used simultaneously, a common problem with single-chip units—particularly the expandable ones. Not really compatible with supplier's Z80 or Z8000 because architecture is so different; closest to Z8000. However, slave Z8 versions interface to Z80 and Z8000 buses. Super8 version has more of everything: more data and program memory, more on-chip peripherals, more instructions.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000

For more information, Circle No. 729

Status: According to Zilog, Z8 volume is still growing and Z8 has had several hundred design wins (many in Far East); some of these design wins are now going into production. Meanwhile, second-source SGS Thomson has turned its CMOS efforts to its ST9, a proprietary enhancement of the Super8, which SGS Thomson uses for an ASIC building block.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram applies to basic 2k-byte version. Many other versions exist.
2. The 124 working registers (272 on Super8) are truly general purpose. Any one can be used as accumulator or indexer.
3. The register pointer singles out a "workspace" of 16 working registers for fast access. Eight such workspaces are possible in the 124-register space (16 in Super8) and provide mechanism for fast context switching upon interrupt.
4. SGS has not announced any CMOS Z8s. Instead it has introduced an S9 ASIC core in 1.5-μm CMOS. According to SGS, this core will reach 12 MHz (24-MHz external clock) and be priced at $4 to $10 in volume.

I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, decimal adjust, increment byte and word, decrement byte and word, subtract, and subtract with borrow.
Multiply and divide added to Super8 version.
Logicals: AND, compare, complement, OR, and exclusive OR.
Rotates and swaps.
Bit manipulation: test under mask, test complement under mask, and logical tests of bits.
II—DATA-MOVEMENT INSTRUCTIONS
Address modes: immediate, register, register pair, indirect register, indirect register pair, direct, indexed, and relative.
Block transfer: load constant autoincrement, load external autoincrement.
Load: clear, load, load constant, load external, and pop and push.
III—PROGRAM-MANIPULATION INSTRUCTIONS
Call, decrement-and-jump on nonzero, interrupt return, jump conditional, jump relative conditional, and return.
IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Set, reset, and complement of carry flag.
Note: Ability to set, reset, and test any bit or combinations of as many as eight bits lets any byte function as a user flag register.

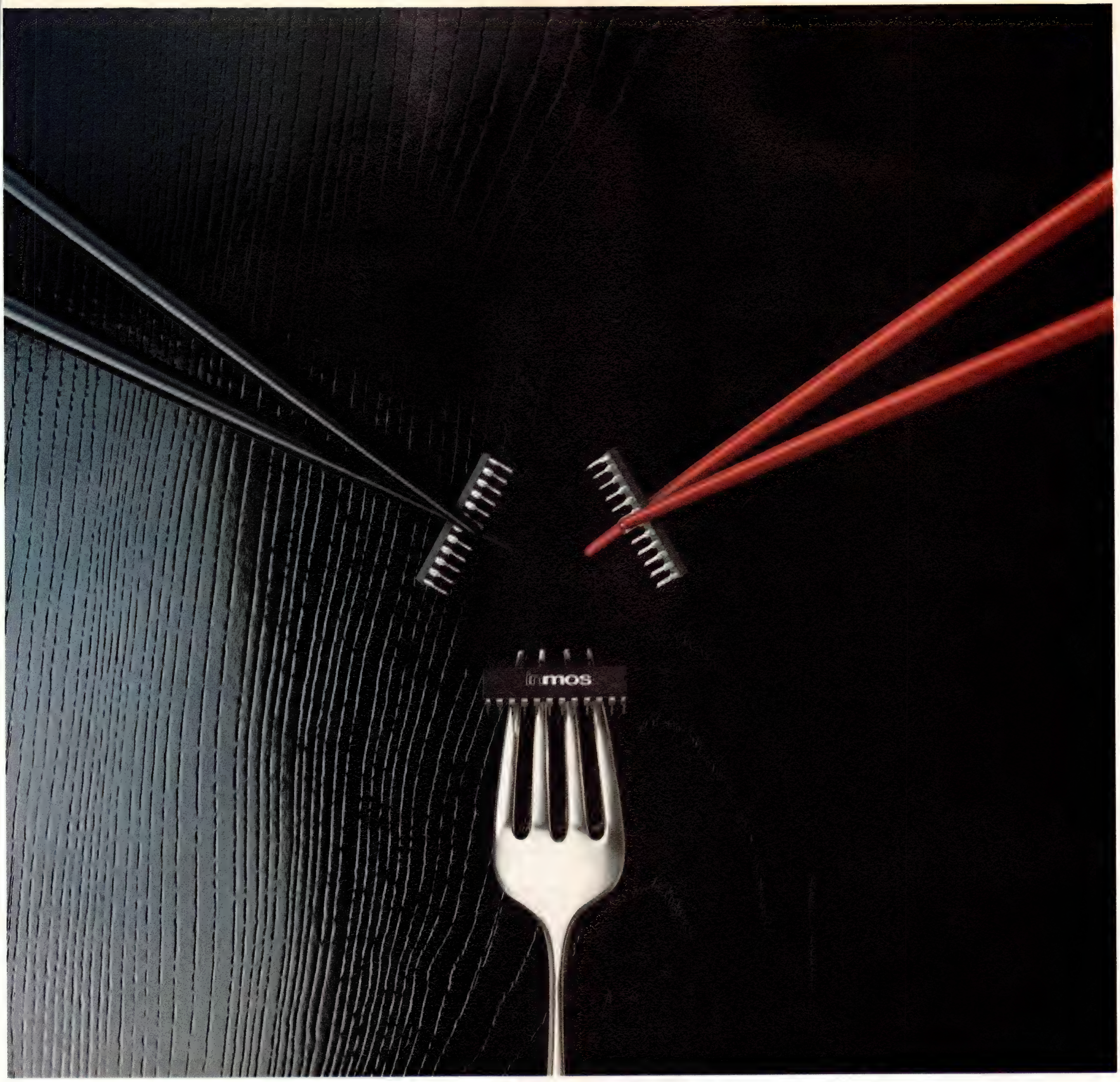
Specification summary: Unique architecture with three memory spaces: program memory (0, 2k, 4k, or 8k bytes in internal masked ROM; rest to 64k bytes can be external), data memory (to 64k bytes external), and CPU register file (256-byte space that includes 124 general-purpose working register/accumulators). Executes 129 instructions at 0.6 to 3.0 μsec at 8-MHz internal clock (16-MHz oscillator). Has built-in duplex UART (96k bps) and two 8-bit timers, each with 6-bit prescaler. Housed in 40-pin DIP; 28-pin economy versions planned. New enhanced Super8 has 352 bytes of on-chip data and control registers, 256 of which are general purpose. Initially it will be a ROMless part, but as much as 16k bytes of on-chip program ROM are expected. New multiply and divide instructions on Super8. Its on-chip peripheral functions include DMA, two 16-bit timer/counters, maximum of 40 I/O lines, full-duplex UART, and optional synchronous/asynchronous serial channel. Has 600-nsec interrupt response with 37 interrupt sources. Available in 48- and 44-pin packages.

Software notes:
1. The data- and program-manipulation instructions use the working registers in the CPU. The instructions that apply to the external data RAM are essentially just loads and stores. (There is a similarity to RISC philosophy.)

HARDWARE — SUPPORT — SOFTWARE

Development packages are available from JK Engineering (Singapore, 65-744-8414). In the US, IAM (Sacramento, CA) distributes JK Engineering's products. Development packages in various configurations are also available from Zilog Inc (Campbell, CA) and Inner Access (Belmont, CA). Emulation packages are available from Orion Instruments (Redwood City, CA), Microtek (Beaverton, OR), Creative Technology (Atlanta, GA), and Sophia Systems (Santa Clara, CA). This list isn't exhaustive.

Software development tools are available from Allen Ashley (Pasadena, CA), Avocet (Rockport, ME), Relational Memory Systems (San Jose, CA), and Western Wares (Norwood, CO). You can purchase compiler software from Micro Computer Compilers (Hopewell, NJ), 2500 AD (Buena Vista, CA), and Inner Access (Belmont, CA). This list isn't exhaustive.



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For those who need large servings of 256K SRAMs, the selection until now has been somewhat limited. The new INMOS 256K SRAM range extends the menu.

The IMS1820 64K × 4 device is available now with an access time of 30ns. From Q1 1990 25ns devices will also be available along with the IMS1800, our 256K × 1 SRAM. Due to investment in new production facilities INMOS is able to supply these devices in quantities to support even the most demanding requirement, and at competitive prices. Just what you'd expect from the largest fast SRAM supplier outside Japan.* These 256K devices join our extensive range of 4K, 16K and 64K fast SRAMs, all of which are available in commercial and military (MIL-STD-883C) versions and manufactured to the highest standards by Europe's leading SRAM manufacturer. For a copy of our Memory Databook or, of course, a quote, contact your local SGS-THOMSON Microelectronics/INMOS office.

inmos

*Source: Dataquest

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CIRCLE NO 61

7000 FAMILY

8-BIT CMOS

AVAILABILITY: Now.
COST: TI pricing: \$1.60 to \$3.50 (100k) for standard CMOS masked-ROM versions.
SECOND SOURCE: Microchip Technology and Seeq for NMOS versions only. Note that each supplier is extending the family in different directions, so direct second sourcing is limited.

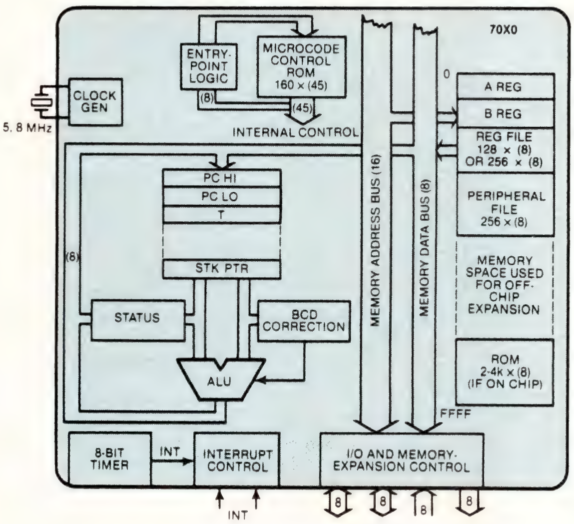
Texas Instruments Inc
Microprocessor and Microcontroller Products Div
Box 809066
Dallas, TX 75380
Phone (800) 232-3200

For more information, Circle No. 733

Description: Software-compatible family of NMOS and CMOS 8-bit, expandable single-chip μCs. Architecture laid out on chip so that new product variations in memory size and I/O are easier to accomplish. A full-duplex UART, enhanced timers, and interrupts are incorporated in high-end family members (70C42). Instructions typically perform combined load, operation, and store functions, thereby increasing overall system performance and code efficiency.

Status: Primary supplier TI has switched its emphasis to CMOS models with expanded features. Low-end devices (70CT20/40) offer an alternative for designers who are using 4-bit μPs but seek a low-cost 8-bit alternative.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware note:
Supplier uses a "strip-chip" architecture to keep registers and control elements in isolated, self-contained modules in silicon, then it uses a single layer of metal to interconnect chip. This approach is similar to the cell-library, semicustom approach and useful for the same reason. Changes can be made easily, which helps TI bring out new models or give large customers special variants.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, 8 × 8-bit multiply, and BCD.
Logicals, increment, and decrement.
Rotates right and left. Bit test.
II—DATA-MOVEMENT INSTRUCTIONS
Dual-operand moves avoid time wasted going through accumulator.
Apply to many instructions.
Indexing via B register.
16-bit moves.
III—PROGRAM-MANIPULATION INSTR
Call and return.
Bit test and jump on both I/O and memory.
Conditonal jumps using PC-relative addressing.
IV—PROGRAM-STATUS-MANIP INSTR
Status register contains carry, sign, zero, and interrupt enable. Instructions to change carry and interrupt enable.

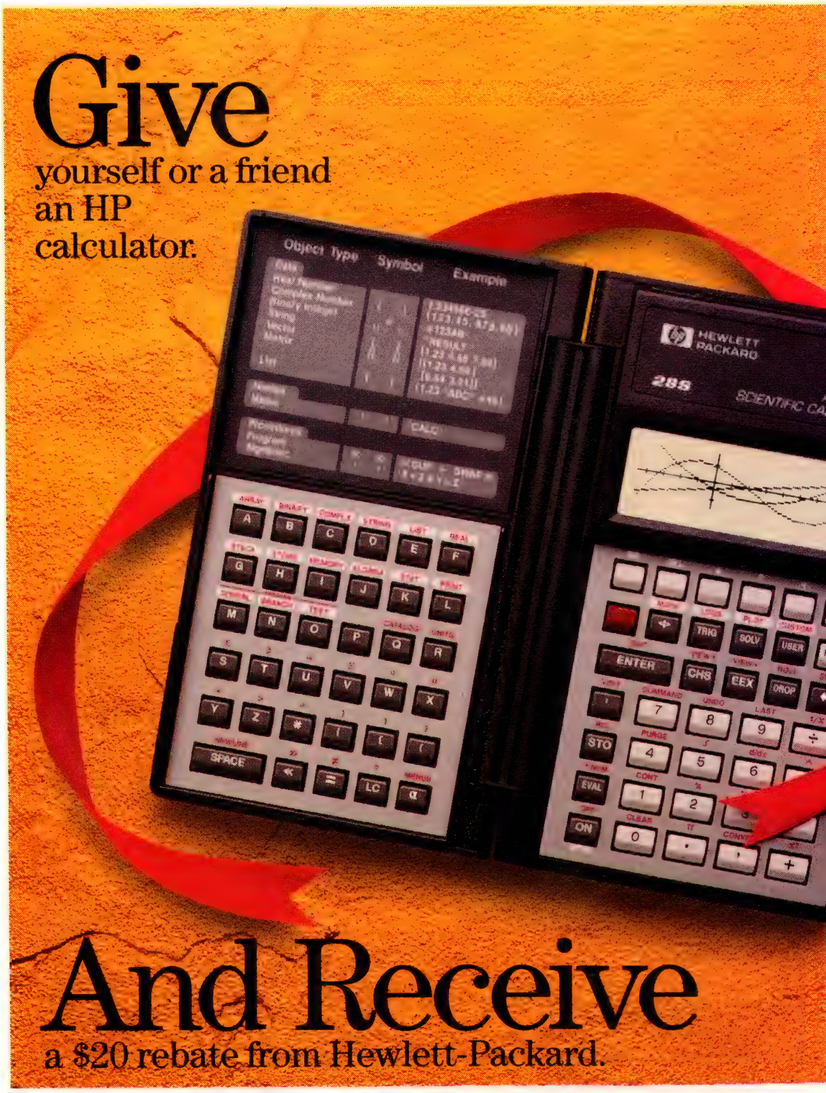
Specification summary: Unified-memory architecture in which application-program ROM (in EPROM), working registers, I/O registers, and some control registers all share common memory space of 64k bytes (except TI 70CTXX models). Low-end family members have 8-bit timer with capture latch and 5-bit prescale; interrupt; 128 and 256 bytes of RAM; and 2k or 4k bytes of ROM. High-end 70C42 includes two 16-bit timers (one with capture latch), which are cascadable to 26 bits; a UART with an 8-bit timer for baud-rate generation (or usable as a third timer); programmable interrupts; 256 bytes of RAM; and 4k bytes of ROM. High-performance model operates to 6 MHz with basic micro-instruction cycle taking 333 nsec. Most instructions take 5 to 9 cycles. Miminum instruction time is 1.25 μsec, which includes load, logic or arithmetic operations, and store. I/O to 32 pins with some models, including special functions such as UARTs and ADCs. NMOS and NMOS-EPROM devices require 5V supplies; CMOS operates over 2.5 to 6V V_{CC} and includes power-down modes. Available in 28- and 40-pin DIPs and 28- and 44-pin PLCCs.

MODEL	ROM (BYTES)	RAM (BYTES)	CLOCK (MHz)	I/O	INTERRUPT LEVELS	POWER REQUIRED V	POWER REQUIRED mW
70C00	0	128	5	32	4	2.5–6.0	30
70C20	2k	128	5	32	4	2.5–6.0	30
70CT20	2k	128	5	20	4	4.5–5.5	30
70C40	4k	128	5	32	4	2.5–6.0	30
70CT40	4k	128	5	20	4	4.5–5.5	30
70C02	0	256	6	32	6	2.5–6.0	30
70C42	4k	256	6	32	6	2.5–6.0	30

HARDWARE — SUPPORT — SOFTWARE

From TI: XDS development system (\$5900). It provides in-circuit emulation, target-system debug (with breakpoints and logic-state trace), and RS-232C link to host computer or terminal. EVM evaluation board (\$795) provides in-circuit emulation, programs SE77C42 and EPROMs, and has serial interface to standard terminals. Piggyback devices accept 27C64 and 27C128 EPROMs. SE70CP160 CMOS piggyback device supports prototyping for 70C20, 70CT20, 70CT40, and 70C40 μCs. SE70CP162 CMOS piggybacking device and SE77C42 support prototyping for 70C42.

From TI: Cross-assembler and linker to run on MS-DOS-based PC that may serve as host for XDS. DEC VAX VMS assembler/linker support is also available.
From Cybernetic Micro Systems (San Gregoria, CA): Assembler, simulator, and debugger to run on IBM PC.
From Allen Ashley (Pasadena, CA): Cross-assemblers and emulators to run on IBM PC.
Literature: TI 7000 family data manual with applications.



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CIRCLE NO 62

8085AH/80C85 — 8-BIT NMOS AND CMOS

AVAILABILITY: Now.
COST: Prices for these older multisourced parts have dropped to $1 and below, with prices as low as $0.65 for volume purchases. CMOS parts, especially faster ones, are more expensive. Radiation-hardened CMOS parts are very expensive ($300 to $800).
SECOND SOURCE: 8085: NEC, Toshiba, Mitsubishi, Siemens, and AMD. 80C85: Oki and Newbridge Microsystems (Calmos) active with Harris supplying nuclear-radiation-hardened CMOS to military and aerospace customers.

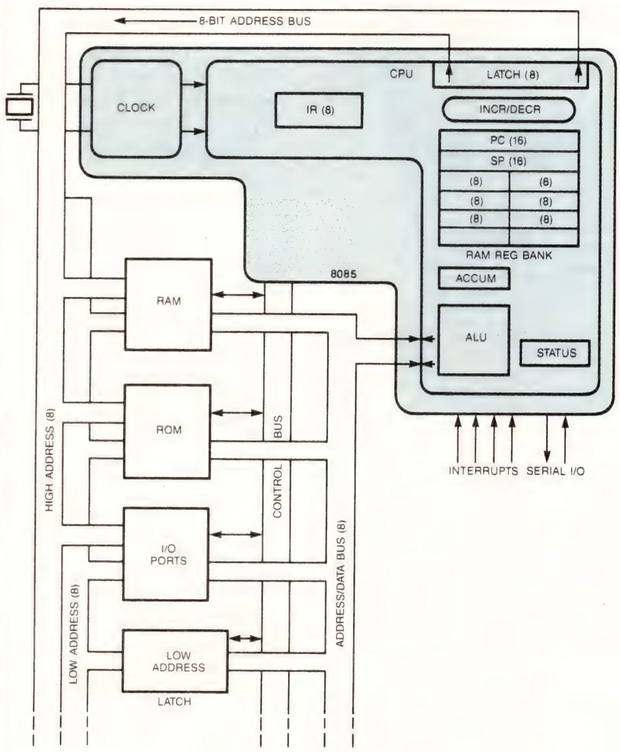
Description: Based on the older 8080 μP, this family has proven a good general-purpose, midrange μP, though not the most efficient one for small programs. 8085 executes 8080 instructions, but with simpler hardware. Z80 (see elsewhere in this directory) is an enhanced 8080 but has different package pinouts and bus operation. New 8086 (see elsewhere in this directory) is only vaguely software compatible, but 8-bit-bus 8088 version of 8086 can interface to 8080 and 8085 peripherals.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

For more information, Circle No. 734

Status: The venerable 8080—the μP that gave legitimacy to the μP revolution—is obsolete. Sales of the 8085 are also falling off, according to Dataquest figures.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
BCD arithmetic.
Double-precision operations (instructions string two data bytes together as 16-bit word).
II—DATA-MOVEMENT INSTRUCTIONS
Uses three pairs of so-called general-purpose registers as pointers in CPU RAM bank to address low- and high-order bits of 16-bit memory address. Can perform multiple indexing with these, but takes additional steps compared with classical index-register concept. 8085 has two additional instructions—RIM and SIM—that interface with new serial-I/O pins and interrupt system.
III—PROGRAM-MANIPULATION INSTR
Uses stack pointer to create LIFO stacks in external RAM for unlimited subroutine nesting.
All GP registers can be incremented and decremented.
Multiple-interrupt capability.
Bus controls allow addition of DMA.
IV—PROGRAM-STATUS-MANIP INSTR
Software access to status register.

Hardware note:
The 8085 differs from the 8080 in that the 8085 has on-chip clock, needs only a 5V supply, and has relaxed memory-access time. But because it multiplexes lower eight bits of address on data bus, it's not pin compatible with 8080. New pins gained by multiplexing implement address-latch strobe, four additional interrupts, and two serial-I/O lines. For small "few-chip" μP systems, a designer can use 8155/56 and 8355/8755 combo chips with built-in address latches.

Specification summary: Common instruction and data architecture (64k bytes) with optionally separate I/O space (256 addresses). Three 16-bit pointer registers allow efficient addressing of 64k-byte main-memory space. 78 basic instructions with 2-μsec (typ) register-to-accumulator addition-execute time. 8085A has on-chip clock and needs only 5V. 5-MHz and CMOS versions of the 8085A available. The Newbridge Microsystems (Calmos) version officially supports the extended 8085 instructions set.

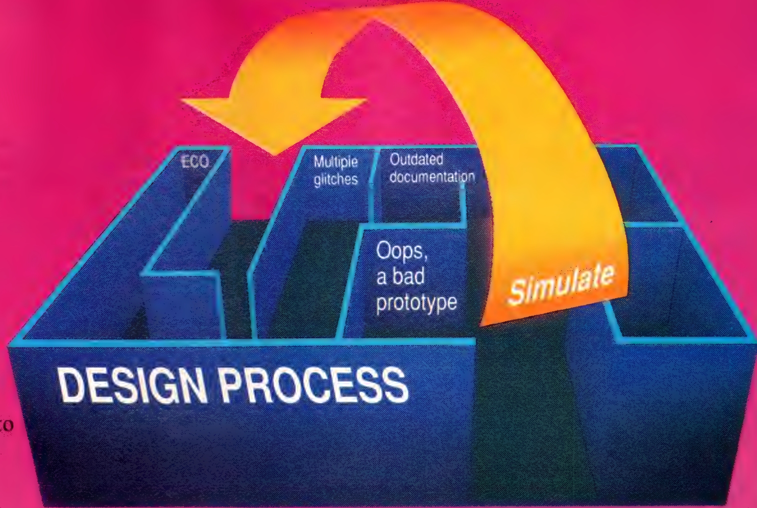
HARDWARE — SUPPORT — SOFTWARE

Most of the vendors of third-party μP development systems have included 8080/8085 development components as a routine part of their catalogs. Typically, these systems use IBM PCs as host.

Most of the many companies that supply 8080/8085 development systems also supply the software. Also, many software houses have 8080/8085 software in every conceivable category.

rCAD Answers Your Questions About

Logic Simulation



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A: To save time.

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A: To make you look good.

Your schematic is supposed to be the best answer to someone else's design problem. Think of how great you'll look when you present a solution with no glitches, timing violations or other problems.

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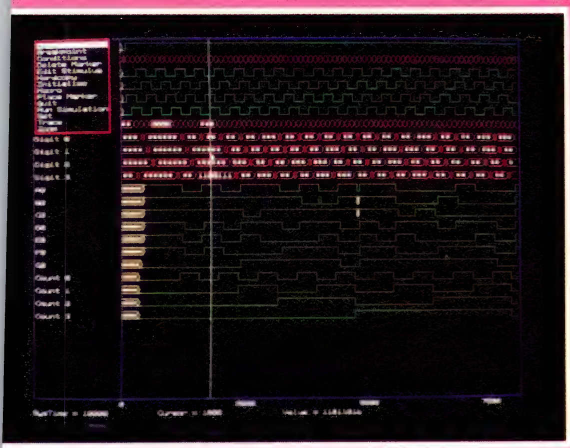

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CIRCLE NO 63

Z80 — 8-BIT NMOS AND CMOS

AVAILABILITY: Now for 6-, 8-, and 10-MHz NMOS and CMOS versions.
COST: Because of the many aggressive second sources for this most widely used part, NMOS prices have dropped to between \$0.80 and \$1.10; CMOS prices have dropped to between \$1.20 and \$1.60 in high volume. The 10-MHz CMOS part costs \$2.50 (100).
SECOND SOURCE: Sharp, SGS Thomson, NEC, and Toshiba. Sharp, SGS Thomson, and Toshiba as well as Zilog have CMOS versions. Additional sources mentioned by Zilog are Gold Star, VLSI Technology, and Rohm.
CORE: Both Zilog and Hitachi are considering the Z80 μP as an ASIC core in their enhanced versions of this core, the 64180 and the Z280.

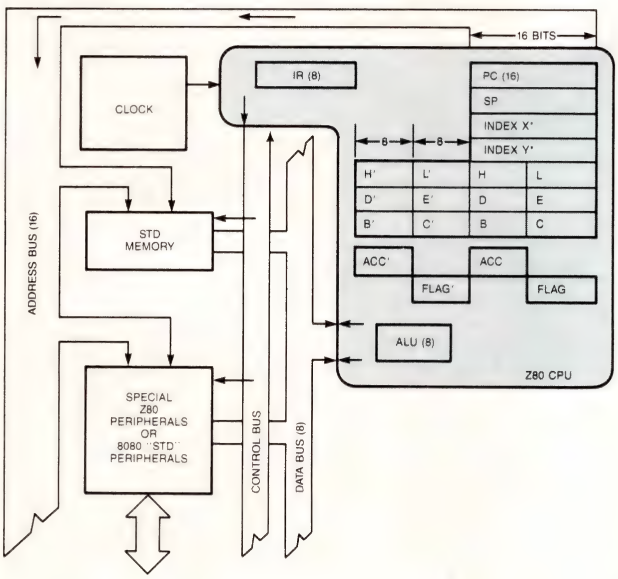
Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000

For more information, Circle No. 735

Description: Superset of widely used 8080/85; adds hardware and software features. Not pin-for-pin compatible with 8080 or 8085 but can use 8080 software and peripherals—although to do so would not take full advantage of Z80 and its peripherals, and it might require additional logic for interfacing. The Z80 and its peripherals are now available in quad flatpacks and all peripherals have been upgraded to run at 10 MHz.

Status: By far the most successful 8-bit μP. The Z80 is still being used in new designs but may be superseded by the new enhanced versions. Of these, the Hitachi 64180 seems to be the most popular, but the Zilog Z280 represents the greatest Z80 enhancement. Whatever happens, one thing is certain: The Z80's momentum will probably last for the rest of this century, especially in ASIC-core form.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Support chips include peripheral interface, timer, serial communications, and DMA. All provide daisy-chained vectored interrupt for CPU and are being converted to CMOS.
2. Several enhancements of Z80 exist or are imminent. All are in CMOS. The first is the Hitachi 64180, to which many Z80 designers are converting. The second is the supplier's Z280, which boosts the Z80 into minicomputer performance. In addition, the NEC 78XX single-chip device is similar. Most are covered elsewhere in this directory.

I—DATA-MANIPULATION INSTRUCTIONS
8-bit arithmetic and logicals.
16-bit arithmetic BCD add and subtract.
Nine types of rotate and shift directly on any register or memory location.
Can set, reset, or test bit in any register or memory location.
II—DATA-MOVEMENT INSTRUCTIONS
8- or 16-bit register or memory loads.
Two index registers allow indexed addressing.
Extensive memory-block move/search commands.
III—PROGRAM-MANIPULATION INSTR
Uses 16-bit stack pointer with LIFO stack with RAM.
Relative-jump capability. Interrupt capability with three types of selectable response.
IV—PROGRAM-STATUS-MANIP INSTR
Seven flag bits, including arithmetic and overflow, can be stored and tested.

Specification summary: Upwardly compatible with 8080A software but adds 50 instructions, some of which are advance block-move and block-search macros. Instructions executed in 0.5 to 1.8 μsec (1.5 μsec avg) for 8-MHz Z80 and 1.0 to 5.5 μsec (2 μsec avg) for 4-MHz Z80A. 6-, 8-, and 10-MHz versions are also available. User can switch between two identical banks of CPU registers for fast response to interrupts. NMOS circuitry requires single-phase clock and one 5V supply at 60 mA for Z80, 90 mA for Z80A. TTL-compatible I/O and built-in automatic-refresh signals for dynamic RAMs. MIL-temperature parts available. CMOS version consumes only 15 mA at 4 MHz and less than 10 μA when in power-down (clock-stopped) mode. Housed in 40-pin DIP. CMOS versions also available in flatpack and PLCC.

HARDWARE — SUPPORT — SOFTWARE

From Zilog: "Z-Scan" emulator boxes that can be used alone or with host computers. Z-Scan-80 provides emulation for the Z80H (\$6695).
From SGS Thomson: UX-8/22 development system based on CP/M and available on two 8-in. floppy disks. Package for full-speed in-circuit emulation.
From others: Some of the many third parties that supply Z80 hardware support are Applied Micro, Boston Systems, Emulogic, Hewlett-Packard, Huntsville Microsystems, Nicolet, Orion, Sophia Systems, Tektronix, and Zax. Contact Zilog for addresses.

From Zilog: Software for the various development systems. Macroassembler with relocatable assembler; linking loader; file-maintenance programs; and resident Basic, Cobol, C, Fortran, and PLZ (Zilog-created language that comes in "lower" level that mixes assembly- and system-language statements with a "higher" C language). Z80 has cross-software package that runs on DEC VAX or Zilog S8000 under Unix.
From SGS Thomson: Software package for UX-8/22, including debugger, disassembler, and tracer.
From others: Software of all sorts, including the venerable CP/M operating system (Digital Research) and the MS/X operating system (from Microsoft), which is popular in Japan. Contact Zilog for names and addresses of several dozen other vendors.

HD 64180, Z180 — 8-BIT CMOS

AVAILABILITY: Now for 6-, 8-, and 10-MHz parts.
COST: For 6-MHz parts, $8 (100) and $7 (1000).
SECOND SOURCE: Zilog.
CORE: Hitachi considers basic 64180 a standard cell for building high-integration µPs and µCs.

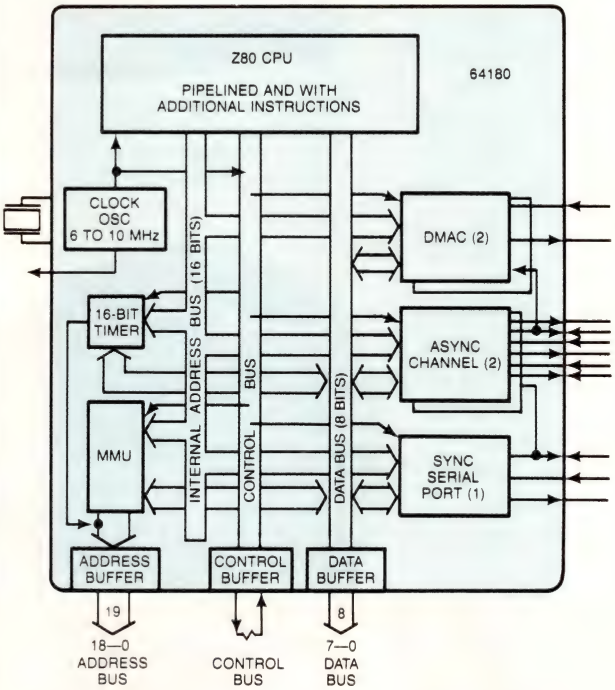
Hitachi America Ltd
Semiconductor and IC Div
2000 Sierra Point Pkwy
Brisbane, CA 94005
Phone (415) 589-8300

Description: Enhancement of Z80 with various peripheral functions such as memory management (to reach larger, 1M-byte, memory space), two DMA channels, two serial ports, and timers added on CMOS CPU chip. Z-suffix versions have total compatibility with Z80-family peripherals chips. Hitachi 647180 with on-chip EPROM represents first single-chip Z80-type µC.

For more information, Circle No. 736

Status: Another CMOS enhancement of the widely used Z80. Has on-chip MMU, multiple DMA channels, and UART like the Zilog Z280, but it's not as ambitious. It doesn't have sophisticated big-computer features such as separate privileged "system" control registers, nor does it have a cache. Moreover, the 64180's MMU is not for virtual and protected memory; it translates between the Z80 64k-byte address space and the 1M-byte space reached externally by the 64180. It has received a boost from all Z80 users and third-party supporters of the venerable Z80.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram is for basic 64180 core. Hitachi plans to expand upon this core.
2. The 647180 is single-chip version of 64180 in which 16k bytes of EPROM and 512 bytes of RAM have been added along with another 16-bit timer, 6-channel analog comparator, and 54 I/O pins. It comes in windowless plastic 84-pin PLCC and 80-pin flatpack. Because of EPROM, Hitachi bills this style µC as a zero-turn-around-time (ZTAT) part, saying it is cost-effective in volumes as great as 5k.

I—DATA-MANIPULATION INSTRUCTIONS
Unsigned 8×8-bit=16-bit multiply.
Nondestructive ANDs for comparing I/O ports, immediate data, and memory to accumulator.
II—DATA-MOVEMENT INSTRUCTIONS
Immediately addressed locations.
Block output to I/O. Must set up MMU bank registers to translate between 64k of Z80 and 512k external.
V—POWER-SAVING INSTRUCTIONS
Sleep command disconnects processor from clock. Interrupt or reset will reconnect.

Software notes:
1. Only new instructions beyond Z80 instructions listed.
2. The MMU adds base registers to Z80 16-bit addresses to produce the 19-bit addresses needed externally.
3. Trap interrupt can be used both for catching undefined op codes and for letting users extend instruction set.

Specification summary: Object-code compatible with Z80 (and 8080, 8085). Pipelined CPU. On-chip MMU generates 19 bits (512k to 1M bytes) external physical address space. 2-channel direct-memory-access controller, 2-channel asynchronous serial port, synchronous (clocked) serial port. Can interface to 8080 or 6800/6500 buses (Z-suffixed versions are matched to Z80-family peripherals). CMOS versions 50 mW at 4-MHz operation; lower power in sleep and halt modes. Packaged in 64-pin DIP and 68-pin PLCC.

HARDWARE — SUPPORT — SOFTWARE

From Hitachi: ASE Adaptive System Emulator ($7000) plus H6805M01S, a 256k-byte memory board for use with IBM PC, HP6400, or DEC VAX as host. Real-time operation as fast as 8 MHz and real-time tracer buffer for 2048 machine cycles. All hardware lines are captured, and the trace is automatically disassembled.
From Others: American Automation AA 572-64180 real-time in-circuit emulator for use with the company's E2-PRO development host.
Hewlett-Packard and Tektronix offer support on their development systems and logic analyzers.
Contact suppliers for the many other third-party vendors.

Microtec Research (Santa Clara, CA) supplies macroassembler, utilities, Pascal, and C compilers (to run on IBM PC and DEC VAX hosts). Avocet (Rockport, ME) and Allen Ashley (Pasadena, CA) have announced IBM PC-based assemblers. Hitachi provides help so that the additional 64180 instructions can be treated as macros on a Z80 macroassembler. Boston Systems Office (Waltham, MA) offers VAX-hosted assembler ($3900). Software compatible with CP/M (Digital Research) and MSX (Microsoft) operating systems (latter being result of project for Japanese market).
American Automation has cross-software to go with development hardware (assembler, C compiler, and debugger).
Archimedes (San Francisco, CA) offers C compiler ($995 for IBM PC; $3995 for MicroVAX; and $5995 for VAX).

AVAILABILITY: Now.
COST: As with other mature μPs, costs have dropped, in this case to a couple of dollars per μP), except when a part is at end of its life, in which case prices might rise again.
SECOND SOURCE: Hitachi, Fujitsu, and SGS Thomson.

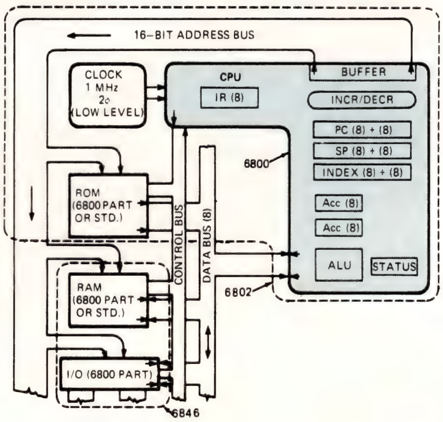
Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 440-2000

For more information, Circle No. 467

Description: The 8-bit 6800 CPU was the original part in the family named after it. That family has been broadened to include not only the 2-chip 6802/6846 and 6809 covered here but also the single-chip 6801, the low-end single-chip devices, and the 6804 and the 6805. Note, however, that new CPU members aren't precisely compatible with the original 6800, especially at the low and high ends. Even the 6809 is only software compatible with the original 6800 at source-code level.

Status: Introduced in 1974, the 6800 has been the foundation of one of the longest lived and broadest μP families of all. Among its progeny are the 6809 covered here and the following Motorola μPs and μCs, which are described elsewhere in this directory: the 6804, 6805, 6801, and 68HC11. The 6800 is now past its prime and is not recommended for new designs; we retain it in the directory for reference. But the newer 6802 and 6809 continue to be shipped in volume. For new designs, Motorola steers designers either upwards to 16- and 32-bit 68000 family (68008 has 8-bit bus) or downwards to the 68HC11.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram shows 6800 and 6802. The 6809 has another 16-bit index and a second "user" stack pointer, which make the 6809 more powerful than the 6800; these additional resources give the 6809 many more instructions. On simple benchmarks, the 6809 is 270% faster than the equivalent-speed 6800, programs in 42% fewer instructions, and uses 33% less code.
2. Basic 6809 version has on-chip clock. A minimum system results with the following parts: 6809, 6810, and 6846. 6809E version has off-chip clock. An early valid-memory-address (VMA) signal on 6809E allows 3-MHz bus operation with a 2-MHz memory. External clock permits multiprocessing.
3. The memory-management unit (6829) allows the 6809 to run 32 concurrent protected tasks per management unit in 2M-byte address space.
4. Hitachi CMOS version (6309) has 2-, 2.5-, and 3-MHz bus timing; the Sync and CWAI instructions allow a low-power sleep mode.

PART	DESCRIPTION	CLOCK SPEED (MHz)	ROM ×(8)	RAM ×(8)	AVAIL	COST (100 QTY)
6800	CPU NEEDS 2 ⌀ CLOCK	1-2	—	—	NOW	$4-$5
6802	CPU, CLOCK & RAM	1-2 (4 MHz EXT)	—	128	NOW	$4-$5
6809	CPU	2	—	—	NOW	$5-$6
6309	CPU CMOS	3	—	—	NOW	$9.50

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Instructions to take advantage of two accumulators.
6809 has unsigned 8×8-bit multiply with 16-bit product.
II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions.
6809 can use four index registers for merging three source blocks into one destination block.
Can autoincrement and autodecrement by 1 or 2 directly and indirectly.
Page zero can be software relocated during program execution, effectively increasing its size.
Indexing uses the "true indexing" relationship between base and offset (0, 5, 8, 16 bits) rather than the 6800 relationship.
Can utilize the user stack for Polish-notation operations or interpretive languages.
III—PROGRAM-MANIPULATION INSTR
Has PDP-11-type branches and conditional branches. Unlimited subroutine nesting via stack pointer addressing LIFO stacks in RAM.
Does not have vectored interrupt but can achieve function with software or with 6828 priority interrupt controller.
6809 has extensive relative addressing with wide reach, which allows creation of position-independent code and opens door to use of off-the-shelf, mass-produced standard firmware in ROMs.
IV—PROGRAM-STATUS-MANIP INSTR
6809 has instructions for manipulating the status register (condition-code register). It may be transferred or exchanged with any 8-bit register or pushed or pulled on either stack; any number of flag bits may be set or cleared in one instruction.
IV—POWER-SAVING INSTRUCTIONS
6309 has SYNC and CWAI to put CMOS CPU in sleep mode. Sync instruction stops μP until it gets go-ahead signal from interrupt line.

Specification summary for 6800: Common-memory architecture with 16-bit (64k-byte) memory space for instructions, data, and I/O; all data 8 bits wide. Instruction set patterned after the PDP-11 mini as closely as possible in shorter word machine with limited CPU registers. Execution times from 2 to 5 μsec. NMOS circuitry requires one 5V supply, 500 mW; housed in 40-pin DIP. Versions with −55 to +125°C range also available.
Specification summary for 6809: An 8-bit machine with extensive 16-bit addressing capability. Has two 16-bit index registers and a 16-bit user stack pointer that can also be software-specified as a third index register. Upwardly compatible with 6800, but only at source-code level. Bus operates at 2 MHz, so basic speed is similar to that of 6800, but greater efficiency of 16-bit addressing increases throughput. Instruction set has 59 mnemonics and seven addressing selections for a total of 1464 instruction-addressing options. Instructions vary in length from 1 to 5 bytes, with register-inherent operations executing in 1 μsec at 2-MHz bus speed (320-nsec memory access). Longest instruction takes 20 cycles. The 6800 direct or page-zero register is retained but can be software relocated anywhere in memory via programmable register. The chip requires one 5V supply. Two versions, each in 40-pin DIP.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: Emulators range from low-cost (hundreds of dollars) boards to HDS-300 system (about $5000) plus personality modules ($5000).
Support systems and OEM boards available from Motorola Semiconductor Div, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-6900 or (602) 438-3500.
From others: Tektronix and Hewlett-Packard development systems support the 6800. Micro Industries (Westerville, OH) says it has acquired an exclusive license to Motorola's "Micromodule" 8-bit boards.

From Motorola: Software can be obtained free for downloading over phone lines by calling (512) 440-3733. The basic assemblers and other tools are for IBM PC.
Two versions of Basic are available for the 6809: Basic-M and Basic09. The latter is designed to be fast and to permit structured programming. A Pascal compiler diskette is available.

Text continued on pg 136

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

ASICs – Choice not compromise

Programming is quick and easy using readily available, third-party design software and programming hardware. For your high-volume production requirements, programming and testing services are available both from TI and authorized distributors.

When low power and reprogrammability are important, an erasable PLD (EPLD) gives you the freedom to make design changes quickly and easily. For high-volume production requirements, EPLDs are also available in one-time-programmable plastic packages.

To move your EPLD design rapidly from concept to silicon, the TI EPLD Development System accepts a variety of entry formats. These include schematic capture, Boolean equations, state-machine diagrams, and truth tables. TI's desktop CAE tool runs on an IBM®-compatible PC-AT™.

FPGAs: Best of two worlds

Like PLDs, FPGAs are user programmable, provide rapid design and debug, are simple to use, and are virtually risk-free. Like masked gate arrays, FPGAs feature high gate densities, high performance, a large number of user-definable I/Os, and a gate array-like design environment.

Currently available are TI's TPC1010A (1200 gates) and the TPC1020A (2000), with higher densities to follow. Unlike PLDs and gate arrays, FPGAs have a unique architecture that allows 100% observability of the internal circuitry. This provides flexibility of design verification, either "in-circuit" or "in the programming box."

The TI Action Logic System (TI-ALS) is a powerful development tool for implementing your FPGA designs while avoiding NRE fees. The TI-ALS accepts designs from popular CAE software packages including Viewlogic™, OrCAD™, Mentor Graphics™, and Valid™ — resident on PC386, Apollo™, and Sun-3™ platforms.

Gate arrays for greater differentiation

For applications requiring higher-density, high-performance ASICs with fast prototype delivery, TI's TGC100 Series 1-micron gate arrays are an excellent choice. Offering gate-array complexities up to 26K gates and 256 I/Os, the TGC100 Series utilizes familiar general-purpose logic libraries. You can define macros and pinouts, as well as specify packages with pin counts up to 256 pins.

A comprehensive design kit provides the information you need to easily implement your gate-array design.

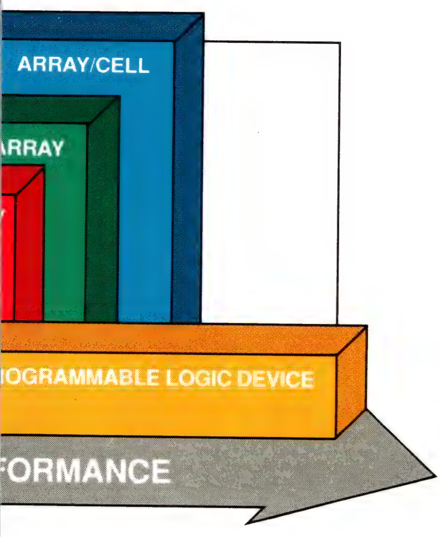
ASIC design centers, located at TI's Regional Technology Centers, are staffed with design specialists who are ready to help you.

Standard cells: As specific, as complex as you need

For ultimate performance and system integration, TI's TSC500 Series is your choice. The extensive cell library contains high-performance memory, register files, FIFOs, and MegaModule™ building blocks. Realizing the need to incorporate design-for-test into today's high-density ASICs, TI also includes JTAG-compatible SCOPE™ testability cells in its library.

Thus, you can tailor a standard-cell design to meet your exact system requirements. As with our gate arrays, a design kit is available, as well as technical design assistance through TI's ASIC design centers.

SPECTRUM



For details about the support and service TI offers, please turn the page.

"I need a high-spe part with unique functionality. Standa architecture is a big priority, too. Plus, I'r going into productio and need volume delivery now."

The TI Solution:

Programmable Logi Devices

At TI, we cover your ASIC needs from silicon to software to service and support.

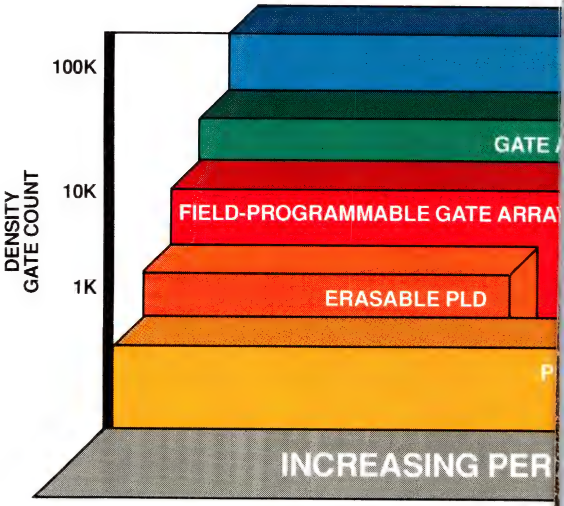
Few ASIC suppliers match TI's breadth of choice and depth of support in helping you develop the most efficient round peg for a round hole. As you see below, our ASIC family spans the architectural spectrum from PLDs to standard cells.

PLDs: High performance, low risk

PLDs are a low-risk, affordable design solution for high-speed-logic consolidation. Stocked on TI distributors' shelves, they allow a quick ramp to volume production.

TI offers more than 40 PLD functions in industry-standard architectures, including the high-speed, 7.5-ns TIBPAL16XX-7 and TIBPAL20XX-7. For high-performance applications, TI also offers unique functions such as the programmable sequence generator, TIBPSG507, and one of industry's fastest programmable address decoders, the 6-ns TIBPAL18N8-6.

TI's ASIC PRODUCT



On my schedule,
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selves. ”

TI Solution:

eld-Programmable
Gate Arrays

“ The system my
team is designing calls
for a high-density, high-
performance ASIC. I
want to call the shots
on pin count, pinout
definition, and the
package itself. Fast
prototype cycle time,
JIT delivery, and low
cost are mandatory. ”

The TI Solution:

Gate Arrays

“ We are developing
a unique product that
requires high-speed
memory and other
complex functions
integrated on the same
chip. Surface-mount,
high-pin-count
packaging is a major
requirement. ”

The TI Solution:

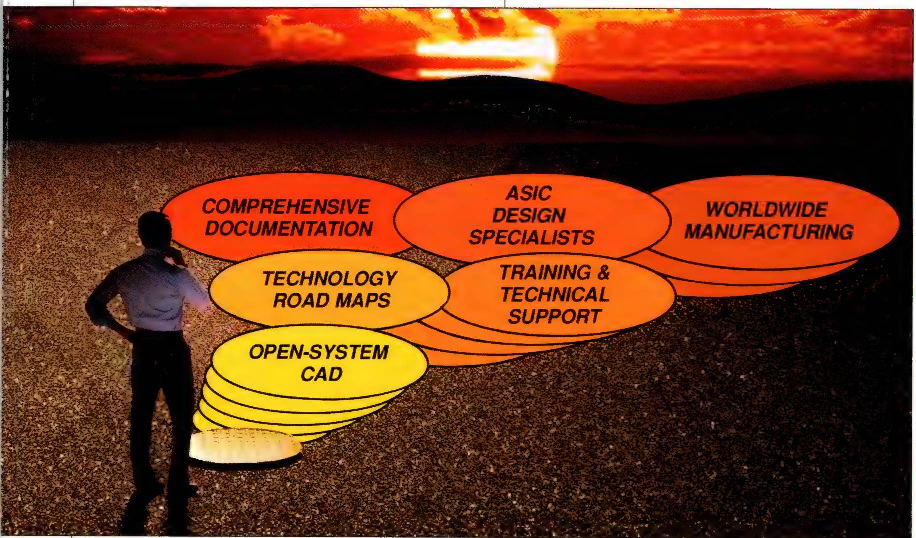
Standard Cells

The sun never sets on TI's service and support.

That's literally true. We have facilities and sites around the world. From early in your design cycle until you have the ASIC solution you envision, TI support and service are available wherever you are.

This around-the-world service and support include that which you have come to expect from TI: Comprehensive documentation and technical literature. Workshop training at our Regional Technology Centers. ASIC design and applications specialists to provide one-on-one advice and counsel. Development hardware and software.

Our design flow is straightforward and minimizes the possibility of surprises.



Our worldwide wafer-fabrication capability is unmatched and moving into the submicron era. We have disclosed a 106K gate array fabricated with our EPIC™-II, 0.8-micron BiCMOS process technology.

Such extensive service and support satisfy the majority of our customers' requirements, resulting in round pegs for round holes. But what if you are one of those whose ASIC solution must be a peg of unusual shape?

Tailoring the "fit"

In these special instances, we will tailor our procedures to your needs, striving to be as "application specific" as the term implies.

For example, certain business issues become very important when a programmable ASIC is best for you. Here, rapidly changing market conditions require absolute supplier dependability.

We can work with you to maintain your inventory levels. We can adapt our production to support your ship-to-stock or just-in-time programs. And if you'd like, we can deliver programmed or unprogrammed PLDs and other ASICs symbolized to your specifications to reduce your internal handling.

We are well aware that an ASIC solution is more than silicon, more than standard service and support.

You may want us to analyze your evolving ASIC designs and needs with you in relation to our evolving technologies. We can "tweak" our design flow to suit your requirements and integrate our design tools within your proprietary CAD systems when required. If your design calls for a proprietary function, we can also create a custom cell to suit your needs.

TI's MegaChip™ Technologies are the means by which we can help you and your company get to market faster with better, more competitive products. Our emphasis on volume manufacturing of high-density circuits is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers.

We at TI are willing to go the extra mile in service and support in order to achieve the ASIC solution best for you.

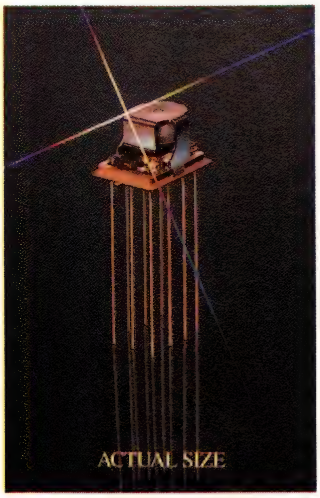
For more information on TI ASICs, call, fax, or write us. **In Europe** call 44-234-223000, fax 44-234-223459, or write Customer Response Centre, MS 09, Texas Instruments Limited, Manton Lane, Bedford MK41 7PA, England. **In Japan** call 81-3-769-8700, fax 81-3-457-6777, or write Texas Instruments Japan Limited, MS Shibaura Building 9F, 4-13-23 Shibaura, Minato-Ku, Tokyo 108, Japan. **In Hong Kong** call 852-3-735-1223, fax 852-3-735-4954, or write Texas Instruments Hong Kong Limited, Market Communications Department, 8th Floor World Shipping Centre, 7 Canton Road, Kowloon, Hong Kong.

TEXAS INSTRUMENTS

TO-5 RELAY TECHNOLOGY

The CMOS Compatible Centigrids®

- Driven directly from CMOS logic
- No amplification or buffering needed
- Fewer components/connections = greater reliability
- Both latching & non-latching versions available



That's right. These little relays are truly CMOS compatible. You can drive them directly with CMOS level signals. No outside amplification at all. An integral power FET driver gives you all the amplification you need. A large Zener diode protects the FET gate input. And all this plus a DPDT relay and coil suppression diode are packed into a tiny Centigrid can.

You can see the advantages up front. Fewer components and connections mean increased reliability. Simpler board layout, too. Add to that the rugged construction and proven contact reliability that have made Centigrid a byword in the industry, and you have a sure winner. One that's QPL approved to MIL-R-28776/7 and 8. One thing more. One version of this little beauty is also a Maglatch. A short pulse of power sets the relay, and it stays that way until it is reset.

No holding power is required. That makes it ideal for applications where power is at a premium. The versatile CMOS compatible Centigrid. It is available in general purpose (116C) sensitive (136C) and Maglatch (122C). Call or write for complete information.

TELEDYNE RELAYS
Innovations In Switching Technology

Teledyne Relays, 12525 Daphne Ave., Hawthorne, California 90250 • (213) 777-0077/**European Headquarters**: W. Germany: Abraham Lincoln Strasse 38-42, 6200 Wiesbaden/Belgium: 181 Chaussee de la Hulpe, 1170 Brussels/U.K.: The Harlequin Centre, Southall Lane, Southall, Middlesex, UB2 5NH/ Japan: Taikoh No. 3 Building, 2-10-7 Shibuya, Shibuya-Ku, Tokyo 150/France: 85-87 Rue Anatole-France, 92300 Levallois-Perret.

CIRCLE NO 66

650X, 65C0X

8-BIT NMOS AND CMOS

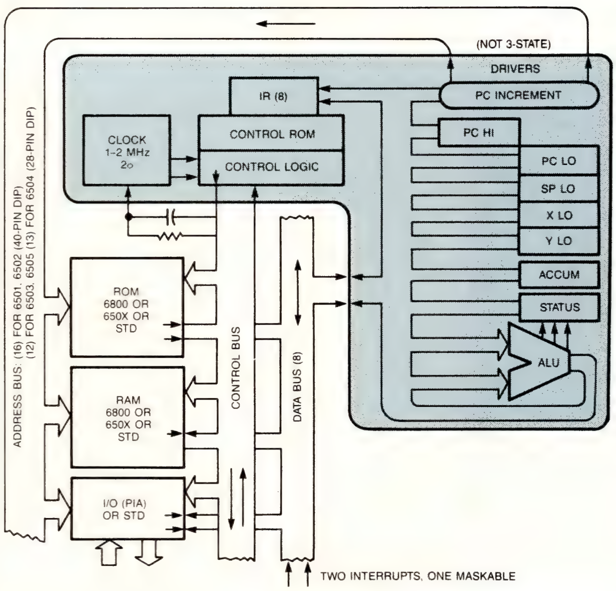
AVAILABILITY: Now.
COST: The prices for both NMOS and CMOS have dropped to less than $1. However "legitimate" US price is $2 to $3 for NMOS and twice that for CMOS.
SECOND SOURCE: Rockwell, California Micro Devices, NCR, and Western Design Center (WDC). WDC created some of the CMOS designs, which it has licensed (UMC in Taiwan, ITT-Intermetall in West Germany), which is one explanation why second sources have proliferated.
CORE: WDC has developed the semicustom 6502 core as NCR and others now use it. Many suppliers now specify it as part of their cell libraries.

Description: Original design team's goal was to achieve as much PDP-11-style addressing capability as would fit in an economical chip. Because of the μP's short 8-bit index registers, it is optimally suited only to applications requiring access of smaller blocks of memory, although it benchmarks ahead of most other 8-bit μPs with respect to its speed of execution of high-level languages such as Basic and Pascal. New CMOS parts also have small economical die that gets still smaller with today's finer geometries. See 6500/1 for single-chip versions and 65SC816/802 for 16-bit-internal version.

Originator Commodore (Westchester, PA) no longer sells chips to the merchant market. Contact second sources.

Status: The falling share of market for this μP appears to indicate that it has reached the end of its lifecycle. However, the architecture lives on in the form of single-chip versions (see 6500/1 and especially the 50740 in this directory) and ASIC versions. Some of these have very large unit volumes, so the 6502 architecture may remain, by volume, the leading 8-bit architecture in the world. WDC is shipping 8-MHz parts and is developing 10-MHz chips.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logical. Decimal mode via control bit in status register. Can operate on locations in memory space, which can be either RAM or I/O ports). CMOS parts have bit manipulation.
II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, although index offset limited to 8 bits in two CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables. CMOS parts have indexed-absolute indirect and zero-page indirect.
III—PROGRAM-MANIPULATION INSTR
Conditional branches with signed relative addresses. Nonmaskable and/or maskable interrupt, depending on model. CMOS parts have branches on bit test.
Stack pointer for implementing 256-byte LIFO in external RAM.
IV—PROGRAM-STATUS-MANIP INSTR
Push and pull status register from memory stack. Set and clear carry, decimal mode and interrupt bits. 6502 and 6512 have external input to one status bit, useful for handshaking with peripherals.
V—POWER-SAVING INSTRUCTIONS
WAIT and STOP on 65C02, respectively, stop processor and disconnect clock to lower power consumption.

Notes on CMOS versions:
1. CMOS 65CXX family members are slight enhancements of NMOS counterparts and can serve as plug-in replacements.
2. Among hardware enhancements are new 4-phase clock that gives decreased memory access time and a memory-lock output and bus-enable input that simplify multiprocessor designs.
3. Among the software enhancements are the treating of all unused op codes as NOPs and removing the page-boundary restrictions on JMP indirect.
4. Decimal mode is automatically set off upon reset or interrupt, and the N, V, and Z flags are made active during decimal mode.
5. A BRK followed by interrupt is executed.
6. See instruction set for comments on new instructions.

Specification summary: Common-memory architecture with instructions, data, and I/O in same 64k-byte space; 57 instructions (68 for CMOS). Many instructions provide choice of 13 PDP-11-type addressing modes (15 for CMOS). Advanced indexed-indirect addressing mode. NMOS and CMOS silicon-gate, depletion-mode circuitry requires one 5V, 250-mV supply. Some CMOS parts can run at 8-MHz clock frequency (125 nsec/cycle). CMOS parts require 4 mA/MHz for operation and 10 μW for standby. Although they supply the μPs in DIPs and PLCCs, WDC recommends using the 44-pin PLCC for higher performance and reliability.

HARDWARE — SUPPORT — SOFTWARE

From Rockwell: LCE emulator ($1250), which interfaces to IBM PC host.
From Western Design Center: Toolbox Design System in-circuit emulator (ICE) runs with an Apple IIGS host and can communicate with an IBM PC via a serial link ($4995).
From California Micro Devices: GEM-I ICE package ($3750) capable of interfacing with a variety of host computers including ISIS development system and Apple. Functions as a stand-alone assembler and disassembler using a nonintelligent terminal. Evaluation board for 65SC150 ($499) that functions as in-circuit system when coupled with GEM-I.
From NCR: Hardware emulator interfaces to Apple IIe through RS-232C port. Allows complete in-circuit software debugging.
From Dynatem (Irvine, CA): AIM-65 single-board computer and RM industrial modules.

From Rockwell: Cross software for Intel ISIS-II and personal development system ($250). Support (in firmware) for assembly ($35), monitor ($65), Basic ($65), PL/65 ($85), Forth ($65), Pascal-"instant" ($100), math package ($35), and disk operating system ($50).
From California Micro Devices: 65SC00 macroassembler for Apple Computer ($100), assembler for Intel ISIS ($1800), and Fortran assembler ($1800).
From NCR: Monitor for use in conjunction with emulator. Supports breakpoint, change memory and registers, software trace, and real-time execution.
From others: Because the 6500 has been so widely used, there are innumerable sources of software at different language levels; for example, Byte Works (Albuquerque, NM), S-C Software (Dallas, TX), Roger-Wagner Publishing (El Cajon, CA), and 2500 AD (Aurora, CO).

8086/8088

8/16-BIT NMOS AND CMOS

AVAILABILITY: Now.
COST: Under $5.50 (1000) for NMOS 8086/88, under $7.50 (1000) for CMOS 8086/88.
SECOND SOURCE: For 8086/8088: AMD, Harris, Matra-Harris, Fujitsu, Siemens, and OKI.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

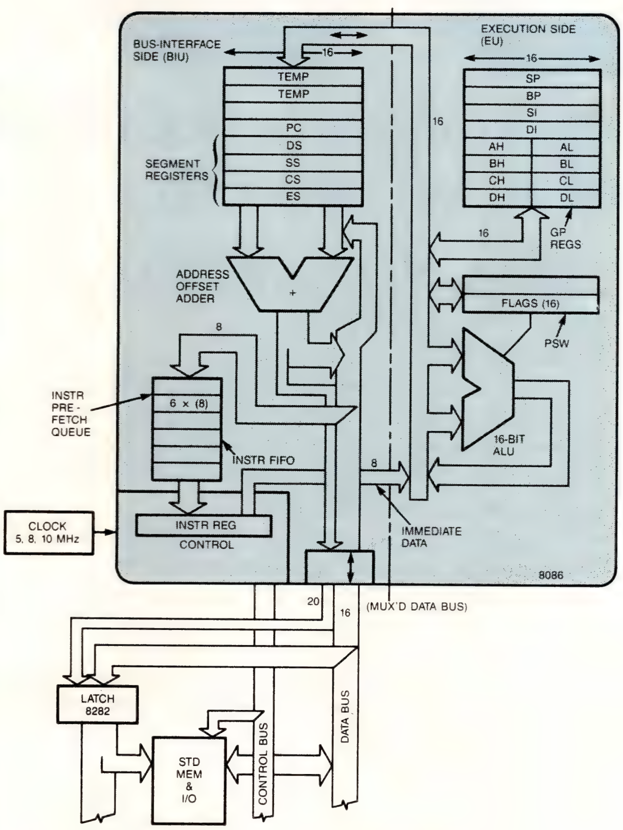
Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

Description: The 8086, 8088, and their low-power CMOS implementations (80C86/80C88) share a 16-bit internal architecture that has a software base of more than 10,000 DOS applications. The 8088 (used in the original IBM PC and its clones) has an 8-bit external data bus to allow the manufacture of lower cost systems with full 16-bit software capability.

For more information, Circle No. 468

Status: Next to the 8080/Z80 family, the 8086 family has been the most successful µP family. Its most visible application has been in the IBM PC and its many clones.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.
Logicals.
Bit, byte, word, and block operations.
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include literal, relative (to register and to segment), register, base-plus index, and base-relative indexed.
Use of segment registers: Programmer can, through software, set up four areas in memory with four segment registers—a program area, a stack area, and two data areas. These areas need not be full 64k, and they can overlap. Programmer can alter the four area locations by modifying the segment-register contents.
III—PROGRAM-MANIPULATION INSTR
Has call, jump, and return instructions both inside program segments and to different segments. Intrasegment call and jump use self-relative displacement for position-independent code. Conditional jump upon Boolean functions of flags within ±128 bytes of instruction. Iteration control of loops, a repeat prefix for rapid iteration in hardware-repeated string operations.
Note: Jumps can occupy varying amounts of execution time, because with BIU's instruction prefetch, the program counter can be ahead of itself
IV—PROGRAM-STATUS-MANIP INSTR
In addition to 8080/85 flags: overflow, interrupt enable, direction (for strings), and single-step trap flags.

Hardware notes:
1. Diagram is for initial family member, 8086.
2. 8088 is downgraded version of 8086. It has only 8-bit-wide external data output bus (only 8 lower bits of address bus are multiplexed for data). Some pin functions have been changed. Prefetch queue is only 4 bytes (to prevent overuse of bus). Instruction execution is slower as all 16-bit fetches and writes take four extra cycles.

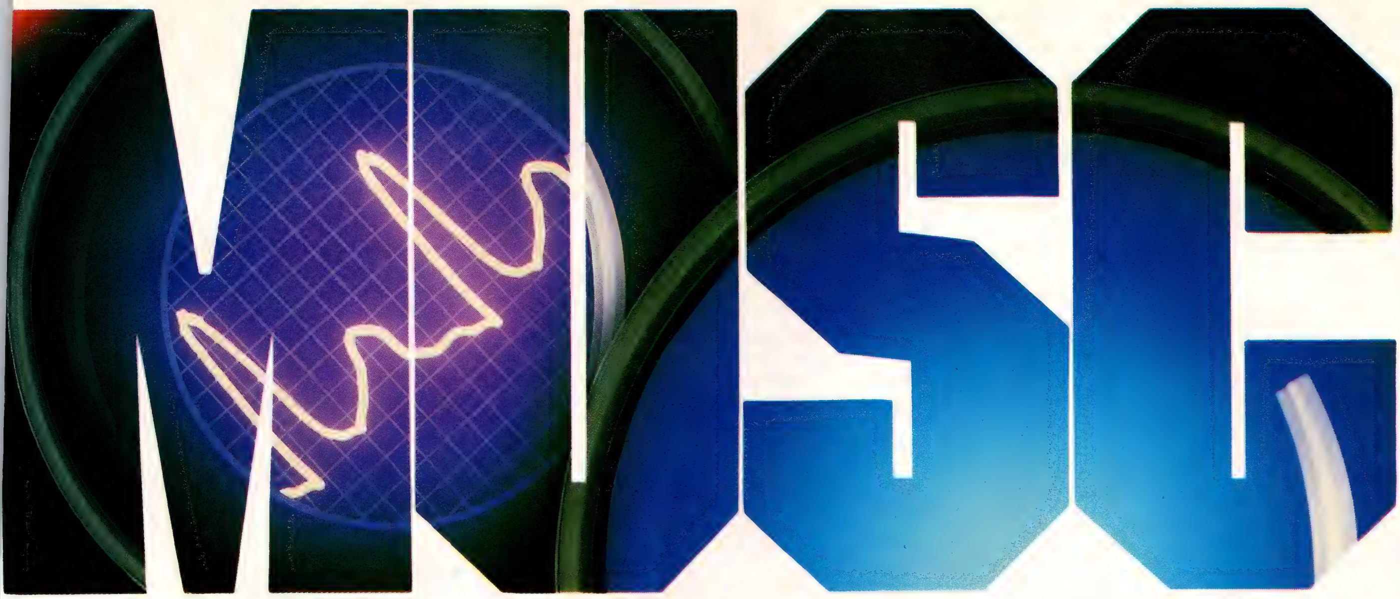
Specification summary for 8086/88: 16-bit CPU that can reach 1M byte using "segment" address-extension registers. Register-to-register operations execute at 0.6 µsec with 5-MHz clock (0.37 µsec with 8-MHz clock). HMOS ion-implanted, depletion-load, silicon-gate circuitry; requires 5V at 340 mA (substrate bias generated on chip). In 40-pin DIP, device is pin programmed to switch eight pins from minimum to maximum external system mode. Harris CMOS 8086 dissipates only 10 mA/MHz when running; clock can be stopped for 500 µA standby.

HARDWARE — SUPPORT — SOFTWARE

From Intel: I²ICE in-circuit emulator ($7995) supports 8086/8088 to 10 MHz. Emulators are hosted on IBM PC and Intellec Series III/IV development systems. All ICEs provide windowed, menu-driven, source-level display and µP debug. Performance Analysis Tool (iPAT) consists of a hardware base unit, an interface to ICE, and host software for the IBM PC/XT and PC/AT. iPAT provides high-level access to target-system performance analysis and test-case code-coverage analysis for the 8086/8088.
From others: Because of popularity, family is widely supported by third-party universal development systems.

From Intel: Macroassembler, including linker, locator, mapper, and librarian. High-level-language compilers include PL/M, C, Fortran, and Pascal. DB-86 software debugger provides windowed, menu-driven, source-level debug with full source-code display. Hosts include PC-DOS and VAX/VMS. Prices start at $750 (for DOS versions).
From others: Because of wide base of 8086/8088-based systems, particularly the IBM PC, there exists third-party software of all sorts, enough to fill whole catalogs. Check with Intel and various trade journals.

Z I L O G

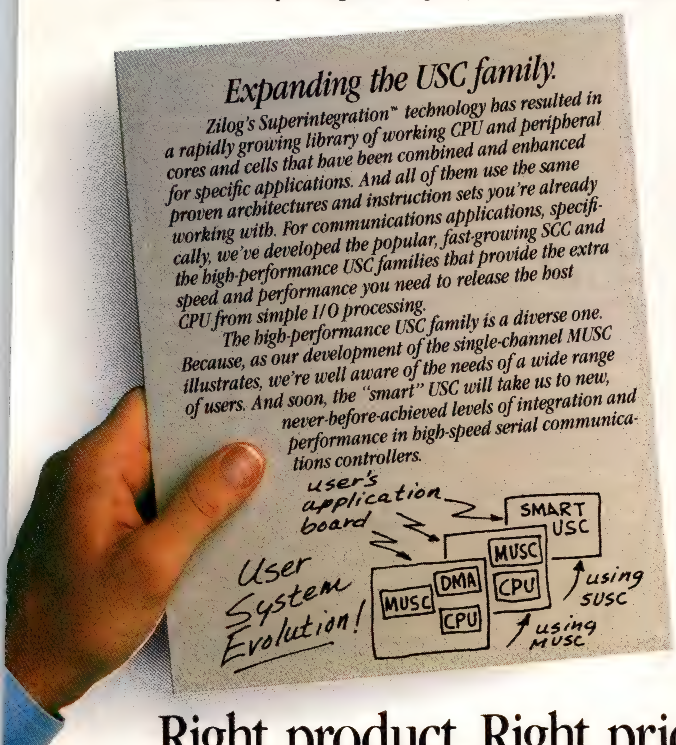


Now you can build 10 Mbit high-performance into your single-channel designs.

Zilog's MUSC, mono-channel universal serial communications controller (Z16C33™), has been designed specifically for high-performance applications that require only one high-speed channel. And it costs you about 40% less than the dual-channel USC.

All the performance you want.

The MUSC's 10 Mbit/sec data transfer rate makes it the fastest single-channel general purpose controller available. CMOS and Superintegration™ give you higher throughput, while helping reduce the CPU workload. And the 32-byte FIFO transmit-and-receive buffers help reduce CPU overhead. So does the fact that the MUSC integrates two time slot assignment cells—one for receive and one for transmit. So data is automatically inserted into programmed time slots, reducing CPU overhead and external logic even more. And all of that frees up more CPU power for the system. The final touch is a separate 8-bit parallel I/O port, ideal for status or displays, that adds flexibility in local control or data presentation.



All the flexibility you need.

The MUSC's multiprotocol design lets you adapt your system to a variety of networks. But not only do you get 10 protocols, you get 8 encoding formats—including asynchronous, bit and byte synchronous, isochronous, Ethernet, and MIL-STD 1553B. And the Open Systems Interconnect (OSI) model features Time Slot Assignment that allows transmission of time multiplexed Synchronous Data Link Control (SDLC) protocol to the ISDN link level.

All the reliability you've come to expect.

Of course, the MUSC comes to you off the shelf, with Zilog's proven quality and reliability. And you have the advantage of CMOS and Superintegration. But you also have the MUSC's unique built-in bus-oriented testability, which allows access to nodes and registers for testing program functionality in real time. And, since dedicated pointer registers provide a window to serial flow during on-line testing, you can test transmission reliability of the controller during system operation.

To find out more about the MUSC or any of Zilog's rapidly growing family of Superintegration products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.

Right product. Right price. Right away.

ZiLOG

ZILOG SALES OFFICES: CA (408) 370-8120, (714) 838-7800, (818) 707-2160, **CO** (303) 494-2905, **FL** (813) 585-2533, **GA** (404) 923-8500, **IL** (312) 517-8080, **NH** (603) 888-8590, **MN** (612) 831-7611, **NJ** (201) 382-5700, **OH** (216) 447-1480, **PA** (215) 653-0230, **TX** (214) 987-9987, **CANADA** Toronto (416) 673-0634, **ENGLAND** Maidenhead (44) (628) 39200, **W. GERMANY** Munich (49) (89) 672045, **JAPAN** Tokyo (81) (3) 587-0528, **HONG KONG** Kowloon (852) (3) 723-8979, **KOREA** (82) (2) 552-5401, **TAIWAN** (886) (2) 741-3125, **SINGAPORE** 65-235 7155, **DISTRIBUTORS: U.S.** Anthem Electronics, Hall-Mark Electronics, JAN Devices, Inc., Schweber Electronics, Vargas Electronics, Western Microtechnology, **CANADA** Future Electronics, SEMAD, **LATIN AMERICA** Argentina—Yel.-(1) 46-2211, Brazil—Digibyte (011) 581-1945.

Z280 — 8/16-BIT CMOS

AVAILABILITY: Now.
COST: About $15 in large volumes.
SECOND SOURCE: None announced, but supplier claims it has strong interest from major European and Far East semiconductor houses.
CORE: Zilog is incorporating elements of Z280 in its megacell library, so it can rapidly put together new combinations. The company claims it can turn around a semicustom design using its megacells in a matter of days. However, it does not plan to offer ASIC tools to customers.

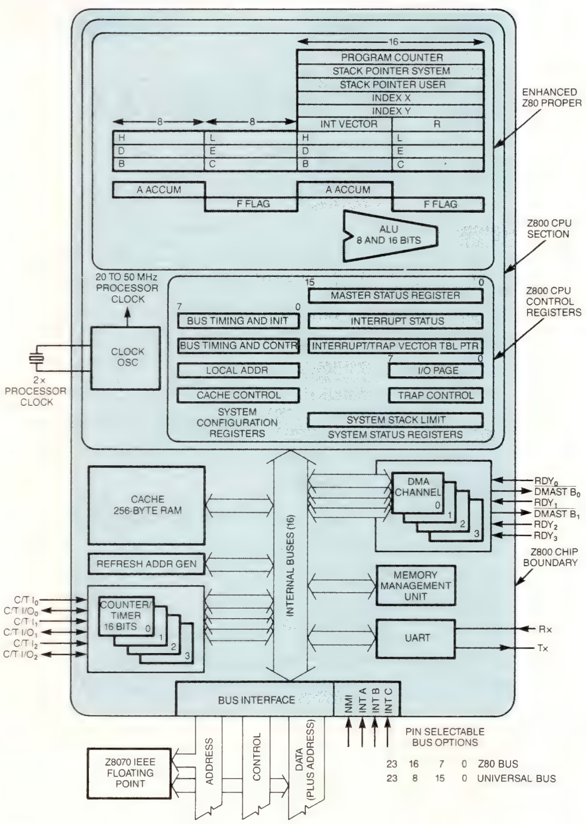
Description: Enhanced Z80 μP, upgraded to the point that it has most of the features of larger 16/32-bit machines. It has "privileged" system-control hardware and associated software for multiuser, multitasking operating systems. It has memory management for virtual memory and incorporates cache to achieve high throughput with moderate-speed external memories.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000

For more information, Circle No. 469

Status: The Z280 became available in late 1987. Basically, the Z280 lets designers upgrade Z80-based personal computers into multiuser systems that have large virtual memories and, claims Zilog, high performance. Zilog says there is a great deal of interest in the Z280, especially in Europe and Japan where Z80-based personal computers have persisted. Compared with other Z80 enhancements, such as the Hitachi 64180 (which Zilog second sources), the Z280 offers a greater performance edge. Zilog is also pushing the Z280 as an upgrade for the many dedicated systems using Z80s as embedded controllers.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram indicates how basic Z80 CPU has been enhanced by adding other functions to the chip. Not so apparent are other enhancements to the Z80 CPU, such as more powerful, generalized 16-bit data and addressing operations.
2. The integration not only lowers system cost but provides a speed advantage: When all subsystems are on chip, the system speed automatically increases.

I—DATA-MANIPULATION INSTRUCTIONS
16 × 16-bit = 32-bit multiply and 32/16-bit = 16-bit divide.
Extended block mode manipulates data in blocks. (Can be used with supplier's Z8070 IEEE floating-point coprocessor).
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes for more general 16-bit use of Z80's 16-bit registers (HL, DE, BC pairs).
Instructions to communicate with coprocessors.
III—PROGRAM-MANIPULATION INSTR
Jump on auxiliary accumulator/flag.
Jump on auxiliary register file in use.
System call.
IV—PROGRAM-STATUS-MANIP INSTR
Master status register; see category V instructions.
V—SYSTEM CONTROL INSTRUCTIONS
Instructions for added system-control registers. These are privileged instructions to permit operating system to define the system configuration upon start-up, to use the new system stack pointer, master status register, and to set up the cache's mode of operation.

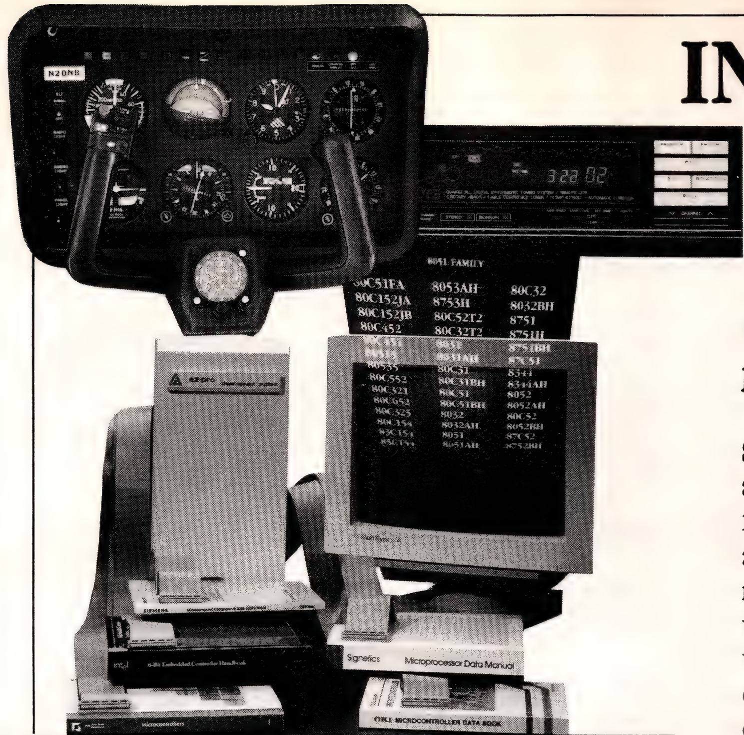
Software note: Only those instructions that are enhancements of basic Z80 set are covered. Otherwise, the Z280 is object-code compatible with Z80 (and 8080).

Specification summary: The Z80 upwardly enhanced toward a general-register 16-bit minicomputer. On-chip memory management to address as many as 16M bytes of external memory. CPU is 3-stage pipelined with on-chip 256-byte program and data cache to automatically keep recently used instruction on chip for fast—to 2 MIPS—execution at 10-MHz internal bus clock. Planned mask shrink from initial 2-μm geometry to 1.5 μm is expected to allow 25-MHz clock. Future mask improvements are expected to allow speeds to 50 MHz. The I/O is pin programmable to match either 8-bit Z80 bus or 16-bit "universal" bus. Also included on chip are four 16-bit timer/counters, four DMA channel controllers, dynamic-memory refresh control, and a serial UART port. The Z280 will be fabricated in static CMOS and housed in 68-pin PLCC; other options planned for future as requested by customers.

HARDWARE — SUPPORT — SOFTWARE

From Zilog: In-circuit-emulator chip and evaluation board.
From others: Softaid (Columbia, MD) has a low-cost real-time development system, and CDS (Statesville, NC) offers evaluation boards for several popular buses. Logic analyzers are sold by Hewlett-Packard and Tektronix.

From Zilog: You can obtain a debug monitor program and a cross-assembler with Zilog's evaluation board. Zilog plans no other software support.
From others: 2500 AD is shipping a cross-assembler and is reported to be working on a C compiler. CDS offers both a cross-assembler and a C complier.



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65C816/65C802 — 8/16-BIT CMOS

AVAILABILITY: Now.
COST: In plastic, $19 (100) for 65C816 and $15.17 (100) for 65C802.
SECOND SOURCE: VLSI and California Micro Devices said to be main sources, but WDC says it has licensed others in US and abroad. (Mitsubishi says it will be making a version of its 50740 6502-based single-chip device that will also have a 16-bit internal architecture.)
CORE: All suppliers are considering this as a μP megacell in their libraries.

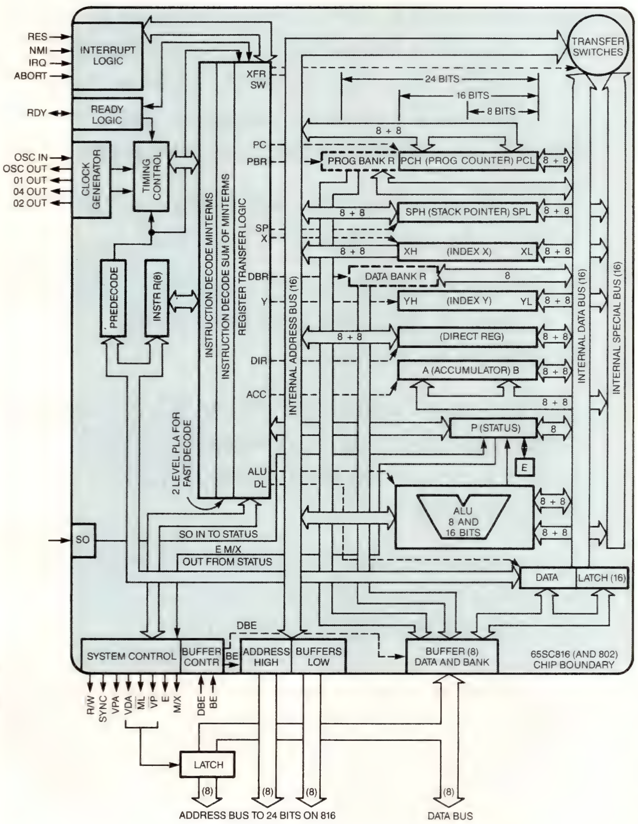
Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
Phone (602) 962-4545

For more information, Circle No. 463

Description: CMOS 8/16-bit μPs featuring software compatibility with 8-bit 6502 (both original NMOS 6502 and enhanced CMOS 65C02). The 802 is pin-for-pin compatible with the 6502, so it can be plugged into existing sockets. The 816 has a different pinout but expands the addressing range of the 6502 from 64k to 16M bytes. Additional hardware enhancements on the 816 allow it to be used for multiprocessor systems and in systems that have data and program caches.

Status: Apple's use of the 65C816 in the IIGS upgrade of the widely used Apple computer provides a firm basis for hardware and software availability. Software support is growing as third-party houses that have supported the 6502-based Apple computers convert software to take advantage of the expanded memory and other capabilities of the 65C816. One indication of breadth of software support is Byte Works' claim that it has delivered several hundred of its software-development tools.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Compare diagram with previous 6502/65SC02 (elsewhere in directory) to see nature of architectural enhancements. The 8-bit registers have been widened to 16 bits, and the 16-bit registers widened to 24 bits.
2. The new control-bus outputs on the 816 facilitate multiprocessing, caching, and virtual memory.
3. The new control-bus inputs on the 816 let you abort instructions for virtual memory as well as control bus access.

I—DATA-MANIPULATION INSTRUCTIONS
The 6502/65C02 instructions with 16-bit versions of add, subtract, BCD, and logicals. No multiply, but future 65C832 version will have provisions for floating point on chip.
II—DATA-MOVEMENT INSTRUCTIONS
6502/65C02 instructions, but with choice of 8- or 16-bit indexing and 8- or 16-bit data widths.
On 816, addressing can span 16M bytes with aid of paging through new register extensions. New block-move (forward or backward) instructions. Increased stack-pointer addressing modes, including stack relative, indirect, and indexed.
III—PROGRAM-MANIPULATION INSTR
Wait for interrupt and stop clock (restart via interrupt). Abort instruction on 816 via pin input acts as interrupt and directs program to perform memory repair and retry.
IV—PROGRAM-STATUS-MANIP INSTR
Additional bits in status register allow software selection of 8- or 16-bit modes for indexing and data. Also, E bit associated with status register (but not handled as part of it) provides software choice of emulation or native mode.

Software notes:
1. Upon reset, 802 and 816 are in 6502 emulation mode. To go to native (enhanced) mode, the E bit must be reset to 0 via an exchange with previously reset carry bit in status register.
2. Full-sized 16-bit registers may facilitate high-level-language compiler writing as compared with 6502. The 16-bit index registers and the 16-bit stack pointer with no page-1 confinement help facilitate compiler writing. Further, the more sophisticated stack-pointer addressing modes directly serve needs of compiler writers.
3. Tendency of native (enhanced) mode coding to become trickier than 6502 due to tightly packed architecture (all 256 op codes used) and opportunity to flip back and forth dynamically between modes and between register and data widths.

Specification summary: Enhanced 6502 with 16-bit internal data option and 24-bit addressing option, software selectable. Data I/O off chip remains 8 bits, however. The 802 version is hardware compatible with 6502 (or 65SC02) and can be plug-in replacement. It will reset into 6502 emulation mode but can be software-switched into varying degrees of 16-bit operation. The 816 version is almost identical internally to 802, but it has different pinouts because it brings the additional bits for 24-bit address space out of the multiplexed 8-bit data bus. The 816 also has special control lines to facilitate virtual memory, coprocessors, and data and program caching. Performance is mostly identical to 6502 of same clock speed, except that extended addressing and data modes take additional cycles. Clock to 8 MHz. Fabricated in 2.4-μm and 1.5-μm CMOS and features 5-mA/MHz power consumption, 1 μA in standby mode. Although it supplies the μPs in DIPs and PLCCs, WDC recommends using the 44-pin PLCC for higher performance and reliability.

HARDWARE — SUPPORT — SOFTWARE

From Western Design Center: The Toolbox Design System in-circuit emulator (ICE) runs with an Apple IIGS host and can communicate with an IBM PC over a serial link ($4995).
From California Micro Devices: Prototyping board for 816.
From Microtek Lab Inc (Gardena, CA): In-circuit emulation system.
From Dynatem (Irvine, CA): RME-1600 board with 65C816.
From Apple (Cupertino, CA): The Apple IIGS personal computer ($700 to $1300) for use as development system because it uses 65C816.

From Byte Works (Albuquerque, NM: The ORCA/M cross-assembly and utility package. C and Pascal compliers are also available.
From Apple (Cupertino, CA): Assembler and debugger ($100) and C compiler.
From others: Supporting products are also available from S-C Software (Dallas, TX); Roger-Wagner Publishing (El Cajon, CA); and 2500 AD (Aurora, CO).

Text continued on pg 146

LINEAR TECHNOLOGY

DESIGN NOTES

Number 28 in a series from Linear Technology Corporation November, 1989

A SPICE Op Amp Macromodel for the LT1012

Walt Jung

Introduction

The Boyle, et al.[1], SPICE macromodel for op amps has proven to be quite useful for fast and efficient computer-based IC circuit analysis, used within its limitations. Critics of this type of model point out that it is not optimum for precise transient analysis of amplifiers using complex compensation. On the other hand, the Boyle macromodel may have little match in terms of the computational speed and performance it can achieve, plus how quickly it can be implemented. These virtues are particularly true for lower frequency op amps, or where DC performance parameters are more important.

The Boyle model can be set up to give realistic and quite reasonable working approximations to a variety of IC op amps which use various types of differential transconductance pair front ends. Two fundamental advantages of this model are the relative simplicity and the simulation speed (particularly when a minimum number of junctions are used). Further, the prudent use of the appropriate transistors at the input can simulate real input offset voltage and bias current effects, as well as such IC-unique features as input common-mode clamping[2], making the overall model much more realistic and akin to real-world ICs. While the original Boyle paper used an NPN bipolar input example (the 741), the topology of the macromodel is also readily adaptable to PNP bipolars as well as JFETs, as design options.

The LT1012

The LT1012 op amp is a popular "universal" high performance internally compensated precision op amp, available in a variety of electrical grades and packages. It uses a rather unique input stage, comprised of a bias current compensated Super-Beta NPN differential pair. This allows the desirably low drift of an NPN pair to be realized, but with typical bias currents of only 30pA, due to the use of both the Super-Beta process and bias current cancellation. Importantly, the low bias currents are *not* achieved at the expense of poor drift and high voltage noise, as the LT1012 (C grade) accomplishes a 1μV/°C Max. drift, and a 14nV/Hz$^{1/2}$ Typ. voltage noise.

The LT1012 has recently been broadened in terms of performance grades, with the addition of a premium "LT1012A" grade part, featuring 25μV Max. V_{OS}, 0.6μV/°C Max. drift, and 500μA Max. supply current. The added "LT1012D" part has a 140μV Max. V_{OS}, a 1.7μV/°C Max. drift, and an 800μA Max. supply current. All device grades have the unusual combination of performance characteristics which allow use as a low-voltage ($\pm$1.2V), low supply current micropower op amp as well as a full $\pm$20V supply range general purpose part. The LT1012 actually exceeds the performance of the industry standard OP-07, doing so at 1/20 the bias/offset currents, and 1/8 of the supply current.

The LT1012 Macromodel

While all of the above may be interesting enough to a designer, how the model imitates the real part is more so. The LT1012 macromodel listed in Figure 1 has a number of features worthy of mention. Note that it is based on the LT1012C room temperature typical specs, taken from the data sheet.

V_{OS}, the input offset voltage of the input pair, is modeled by using two slightly different NPN transistor models, qm1 and qm2. The ratio of their two saturation currents will produce an offset voltage, which is:

$$V_{OS} = KT/q \ln(Is1/Is2)$$

With the ratio as shown, this produces the typical 10μV offset for the LT1012C.

Bias and offset currents are modeled by using a different Bf for the two input pair halves, as:

$$Bf1 = Ic1/Ib1 \text{ and } Bf2 = Ic2/Ib2$$

The Bf values shown for qm1 and qm2 are those which correspond to $Ib = 30pA$; $I_{OS} = 20pA$. While the gains listed are enormously high (even for Super-Beta transistors) this is not a problem for SPICE, so bias currents in the range of a typical LT1012C are produced.

Other additions to the generic Boyle macromodel are the optional input diode clamps, ddm1 and ddm2, as in the real part (they can be deleted, if not used). The substitution of a current source, Ip, in the place of the Rp of the original model simulates quiescent power supply current. The LT1012, like many modern day ICs, has a quiescent supply current which is quite constant with supply voltage, thus Ip is more appropriate than a fixed resistor.

The remaining specifications modeled are shown at the head of the listing, consistent with the LT1012C. The model can also be used for the LT1024 (dual LT1012), if the "x" call is added at the end as shown. A sample small signal pulse response waveform of the model is shown in Figure 2, which can be compared to the similar condition scope photo, from the LT1012 data sheet (pg. 7).

```
*
* Linear Technology LT1012 op amp model (with calls for LT1024)
* Written: 08-17-1989 10:16:25 Type: Bipolar npn input, internal comp.
* Typical specs:
* Vos=1.0E-05, Ib=3.0E-11, Ios=2.0E-11, GBP=6.0E+05Hz, Phase mar.= 70 deg,
* SR(+)=2.0E-01V/us, SR(-)=1.9E-01V/us, Av= 126 dB, CMMR= 132 dB,
* Vsat(+)= 1 V, Vsat(-)= 1 V, Isc=+/- 12.5 mA, Iq= 380 uA
* (input differential mode clamp active)
*
* Connections: + - V+V-O
.subckt LT1012 3 2 7 4 6
* input
rc1 7  80 8.842E+03
rc2 7  90 8.842E+03
q1  80 2  10 qm1
q2  90 3  11 qm2
ddm1 2  3  dm2
ddm2 3  2  dm2
c1  80 90 5.460E-12
re1 10 12 2.246E+02
re2 11 12 2.246E+02
iee 12 4  6.000E-06
re  12 0  3.333E+07
ce  12 0  1.579E-12
* intermediate
gcm 0  8  12 0  2.841E-11
ga  8  0  80 90 1.131E-04
r2  8  0  1.000E+05
c2  1  8  3.000E-11
gb  1  0  8  0  1.960E+02
* output
ro1 1  6  1.000E+02
ro2 1  0  9.000E+02
rc  17 0  1.063E-04
gc  0  17 6  0  9.408E+03
d1  1  17 dm1
d2  17 1  dm1
d3  6  13 dm2
d4  14 6  dm2
vc  7  13 1.785E+00
ve  14 4  1.785E+00
ip  7  4  3.740E-04
dsub 4  7  dm2
* models
.model qm1 npn (is=8.000E-16 bf=7.500E+04)
.model qm2 npn (is=8.003E-16 bf=1.500E+05)
.model dm1 d   (is=1.179E-19)
.model dm2 d   (is=8.000E-16)
.ends LT1012
*
.subckt LT1024 3 2 7 4 6
x_LT1024  3 2 7 4 6 LT1012
.ends  LT1024
*
* - - - - - * fini LT1012 family * - - - - - * [oamm vn1 8/89]
```

Figure 1.

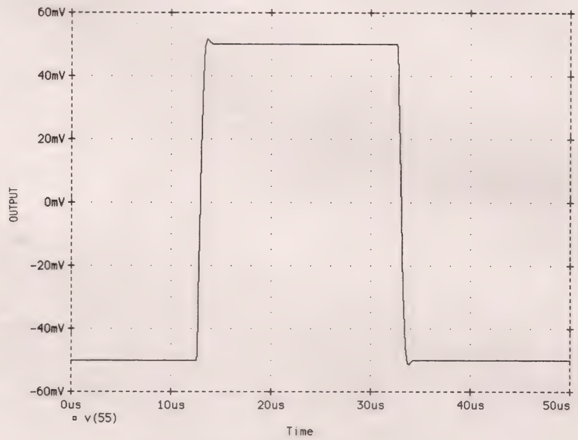


Figure 2. Small Signal Transient Response

References

1. Boyle, G.R., Cohn, B.M., Pederson, D.O., Solomon, J.E., "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, #6, December 1974.
2. Jung, W.G., "An LT1013 Op Amp Macromodel," Linear Technology Design Note Number 13, July 1988.

Obtaining This Macromodel

This model can be entered onto a given computer type simply by typing it in (very carefully!) using an ASCII text editor. Optionally, interested readers may contact LTC at the address or phone number below, for a copy of a PC data disc containing the most recent collection of macromodels (including this model and all those previously released).

For literature on the LT1012 op amp, or a 5 ¼" macromodel disk, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487 • (408) 432-1900
FAX: (408) 434-0507 • TELEX: 499-3977

IM/GP 1089 165K

80186/80188

8/16-BIT NMOS AND CMOS

AVAILABILITY: Now for 8-MHz 80186/188. Now for 10-, 12.5-, and 16-MHz 80C186.
COST: Under $10 (100) for 80186/188 in PLCC. Under $18 for 10-MHz 80C186/C188 in PLCC.
SECOND SOURCE: AMD, Fujitsu, and Siemens.
CORE: Intel's ASIC group plans to incorporate the 80C186 in its cell library.

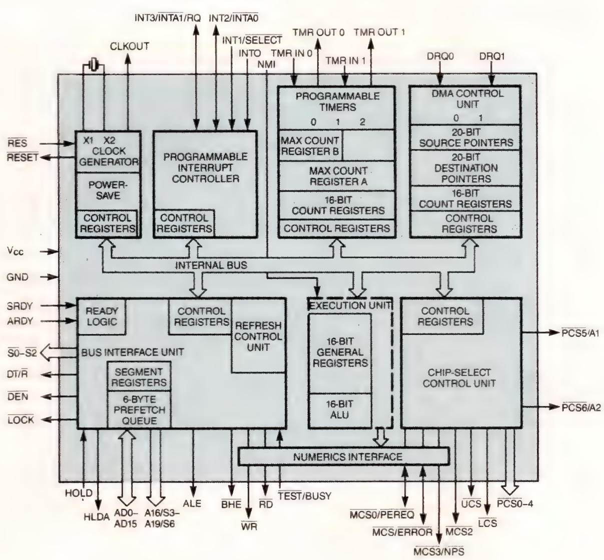
Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

For more information, Circle No. 464

Description: The 80186, 80188, 80C186, and 80C188 are high-performance, highly integrated μPs, that were developed from the 8086 base architecture. The 80186 family of products are completely upward compatible with the 8086 object code and contain 10 additional instructions. These high-performance embedded microprocessors integrate many common system components onto a single chip. This compaction results in increased performance and reliability as well as decreased board space requirements. The onboard peripherals include a clock generator, two independent DMA channels, a programmable interrupt controller, three programmable 16-bit timers, programmable memory, peripheral chip-select logic, and a programmable wait-state generator. Further enhancements to 80C186/C188 products include a power-save mode, a DRAM-refresh control unit, and a direct numerics interface.

Status: The 80C186 family of products is widely used in more than 3500 diverse customer applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Includes addition, subtraction, multiplication, and division. Arithmetic operations may be performed on four types of numbers: unsigned binary, signed binary (integers), unsigned packed decimal, and unsigned unpacked decimal. Binary numbers may be 8 or 16 bits long. Decimal numbers are stored in bytes: two digits per byte for packed decimal, and one digit per byte for unpacked decimal.
II—DATA-MOVEMENT INSTRUCTIONS
Data-transfer instructions move single bytes, words, and double words between memory and registers, as well as between register AL or AX and I/O ports. Stack manipulation instructions are also included, as are instructions for transferring flag contents and for loading segment registers. Subgroups of the data transfer instructions are general-purpose data, I/O, address-object, and flag-transfer instructions.
III—PROGRAM-MANIPULATION INSTR
Includes unconditional transfers, conditional transfers, iteration controls, and interrupts. Unconditional transfers include CALL, JUMP, and RETURN instructions, which may transfer control to a target instruction within the current code segment (intersegment transfer). The conditional transfer instructions are JUMPS that may or may not transfer control, depending on the state of the CPU flags at the time the instruction is executed. You can use the iteration control instructions to regulate the repetition of software loops. The interrupt instructions let programs as well as external hardware devices activate interrupt-service routines.
IV—PROGRAM-STATUS-MANIP INSTR
FLAG operations include carry, direction, and interrupt enable, all of which let programs control various CPU functions.
V—SYSTEM-LEVEL INSTRUCTIONS
The processor controls instructions responsible for external synchronization, which include halt, wait, escape, and lock.

Hardware notes:
1. Diagram is for 80C186.
2. The 80C188 is the 8-bit external-data-bus version of the 80C186. The 80C188 has all other 80C186 features except for the numerics interface.
3. The 80186 and 80188 do not have the DRAM-refresh control unit, power-save mode, or the direct numerics interface.
4. The 8087 math coprocessor supports the 80186/188; the 80C187 supports the 80C186.

Specification summary: 16-bit CPU with direct-addressing capability to 1M-byte memory and 64k-byte I/O with six address modes. There are 14 16-bit registers. Register-to-register operations execute at 125 nsec for the 16-MHz device. The typical current for the 80186/188 at 5V is 320 mA; that for the 80C186/C188 running at 16 MHz is 105 mA. These parts are offered in 68-pin PGAs, LCCs, and PLCCs.

HARDWARE — SUPPORT — SOFTWARE

From Intel: I²ICE186 in-circuit emulator ($8500) supports 80186/188 to 10 MHz. ICE186 in-circuit emulator ($9995) supports 80186/188/C186/C188 for CPUs as fast as 16 MHz. Emulators are hosted on IBM PC and Intellec Series III/IV development systems.
From others: Because of popularity, family is widely supported by third-party universal development systems.

From Intel: Macroassembler, including linker, locator, mapper, and librarian. High-level-language compilers include PL/M, C, Fortran, and Pascal. iPAT performance analysis tool enables the analysis of real-time software execution in prototype systems. Analysis is performed symbolically, nonintrusively, and in real time with 100% sampling in the microprocessor prototype environment.
From others: Because of wide base of 8086- and 8088-based systems, in particular the IBM PC, there is third-party software of all sorts, enough to fill whole catalogs. Check with Intel and various trade journals.

AVAILABILITY: Now for 8, 10, and 12.5-MHz devices; now for 16-and 20-MHz versions from AMD and Harris. Now for CMOS 12.5-MHz 80C286.
COST: $14 (1000) for 8-MHz device; $29 (1000) for 12.5-MHz device. $50 (1000) for 12.5-MHz 80C286.
SECOND SOURCE: AMD, Siemens, and Fujitsu. Harris for CMOS 80C286.

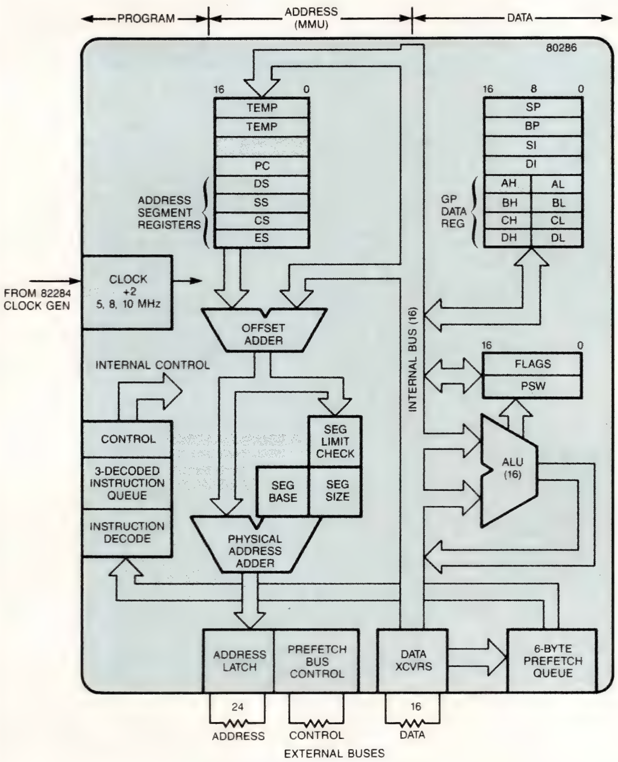
Description: The 80286 is upward compatible with the 8086 and 80188 and includes on-chip memory management and hardware support for multiuser, multitasking systems. A 4-level protection model provides task/task and user/operating-system protection. The 8-MHz 80286 is six times faster than the 5-MHz 8086 due to its pipelined architecture, 8M-byte/sec bus and 3.5-nsec interrupt time. Used in the IBM PC/AT and its clones.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

For more information, Circle No. 465

Status: Intel has de-emphasized the 80286 in favor of its 32-bit siblings, the 80386SX, 80386, and 80486. However, in spite of very low growth, the 80286 still has the highest volume in the 8086 family. Its popularity has been based on the IBM PC/AT. Certainly the second sources will give the 80286 as long and thriving a life as they can, since Intel has shown no inclination to ever let them second source the 80386. Therefore, expect more enhanced 80286s, such as the 16- and 20-MHz versions from AMD and the CMOS version from Harris. Unfortunately for the second sources, the 80286's big sisters, the 80386SX, 80386, and 80486, are taking over many of its applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.
Logical operations on bytes, words, and blocks.
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include literal, relative (to register and to segment), register, base plus index, base relative indexed, and register indirect.
Programmers can manipulate 16,383 segments in memory by means of memory-base descriptor tables and 4-segment registers. These segments can be between 1k and 64k bytes in length.
III—PROGRAM-MANIPULATION INSTR
Has calls, jumps, and returns within the same protection level, across protection boundaries, and between tasks.
Intrasegment calls and jumps use self-relative displacement for position-independent code.
Intersegment calls and jumps use the memory-based descriptor tables to provide position independence of code.
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction.
Iteration control of loops.
String instructions, including repeat, for rapid iteration.
IV—PROGRAM-STATUS-MANIP INSTR
8085 flags (carry, auxiliary carry, parity, zero, and sign) plus overflow, interrupt enable, direction (strings), trap (single-step), I/O privilege level, and nested task. Flag register is software accessible.

Software notes:
1. Has high-level-language support instructions.
2. Virtual-address translation, memory management, and protection performed by CPU for faster execution.
3. Trusted instructions can only be executed at highest protection levels.

Hardware notes:
1. Support chips for 80286: 82C284 clock, 82288 bus controller, 80287 floating-point numeric processor ($187.15 (1000) for 10-MHz version), and 82258 advanced DMA coprocessor.
2. A trend is for third-party VLSI houses to do high-integration chip sets to consolidate the devices being used around popular compute engines, which for the 80286 would be the IBM PC/AT. Chip sets for the IBM PC/AT are being offered by Chips and Technologies (San Jose, CA), Zymos (Sunnyvale, CA), VLSI Technology (Phoenix, AZ), Hudson & Supinger (Santa Clara, CA), Capital Equipment Corp (Burlington, MA), and Via Technologies Inc (Sunnyvale, CA)—as well as by Intel.

Specification summary: 16-bit CPU with 1G-byte virtual-address space per user, mapped onto 16M-byte physical-address space. Bus cycles execute in 250 nsec at 8-MHz clock frequency (200 nsec at 10 MHz), requiring 0.25 μsec for register-to-register moves at 8-MHz clock frequency, with 8M-byte/sec bus bandwidth. HMOS ion-implanted, silicon-gate circuitry in a large chip (335×339 mils, approximately 134,000 transistors). Requires 5V at 600 mA. Has two operating modes: Real-address mode emulates 8086; protected virtual-address mode native to 80286. Housed in a 68-pin JEDEC type-A LCC, PLCC, and PGA.

HARDWARE — SUPPORT — SOFTWARE

From Intel: I²ICE-286 in-circuit emulator ($9995) supports 80286 at 8 and 10 MHz. It is hosted on IBM PC/AT and PC/XT. ICE286 ($12,495) supports 80286 at 12.5 MHz. iPAT Performance Analysis Tool includes a hardware base unit, an interface to ICE, and host software for the IBM PC/AT and PC/XT. iPAT provides high-level access to target-system performance analysis and test-case code-coverage analysis for the 80286 in real and protected mode.
From others: A number of third parties support the 80286 on their universal development systems.

From Intel: Macroassembler (ASM 286), which includes systems builder, binder, mapper, and librarian. Compilers for C, Pascal, PL/M, and Fortran. For applications running in virtual 8086 mode, any of Intel's 8086 software tools can be used. Hosts include PC-DOS and VAX/VMS. $750 for DOS version. Real-time operating systems (Intel's iRMX 286) available.
From others: Other operating systems and compilers being developed by third-party software houses include MP/M-286 (Digital Research), Xenix-286 (Microsoft), Coherent 286 (Mark Williams), Concurrent DOS (Digital Research), Unix System V (Digital Research), and OS/2 by Microsoft (Redmond, WA).

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8096 FAMILY

16-BIT NMOS AND CMOS

AVAILABILITY: Now for NMOS 8096 family. The 8098 chip offers an 8-bit external bus. The EPROM version is also available as is the higher-performance 80C196 CMOS version.
COST: Less than $8 (10k).
SECOND SOURCE: Signetics/Philips.

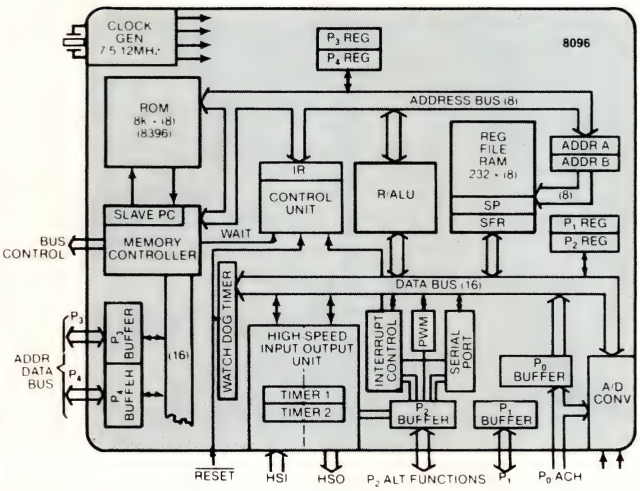
Intel Corp
Chandler Microcontroller and ASIC Div
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

For more information, Circle No. 466

Description: Highly integrated 16-bit microcontroller combining 16-bit CPU with extensive I/O handling. On-chip memory includes 8k bytes of ROM and 232 bytes of register-file RAM. I/O capabilities include an 8-channel, 10-bit ADC, full-duplex UART, 8-level priority interrupt, pulse-width-modulated output, high-speed pulsed I/O, four 16-bit software timers, five 8-bit I/O ports, and a watchdog timer.

Status: This earliest of the 16-bit microcontrollers continues to have a large share of 16-bit market. However, because that market is still young, it's too early to tell whether this will be another case of Intel dominance. National Semiconductor's 16040 and NEC's 783XX (78312), which are newer designs, are being aggressively marketed and could pose threats. Actually, with the growing popularity of ASICs, the definition of this market is blurring; for now, any µP that is in core form in an ASIC library could have memory added and become a "µC," even Intel's own 80188/186.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. The initial NMOS 8096 family consists of parts that come with or without A/D converters, S/H circuits, and onboard ROM, and with either 48 I/O lines (68-pin package) or 32 I/O lines (48-pin package). The family has option of either 8- or 16-bit system bus. The 8098 offers an external 8-bit bus. The 8k-byte EPROM version has onboard programming capability and read/write selectivity.
2. New CMOS version 80C196 has twice NMOS performance.
3. Four high-speed trigger inputs record times at which external events occur. Storage in 8-deep FIFO memory.
4. Six high-speed pulse outputs can trigger external events at preset times. Commands are stored in 8-byte-deep content-addressable memory. Output section can run as many as four software timers simultaneously.
5. 16-bit watchdog timer allows recovery from hardware or software error.

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary, including multiply and divide.
Logicals.
Bit, byte, word, and double-word operations.
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include direct, immediate, indirect, indexed, and indirect with autoincrement.
Load and store, push and pop.
III—PROGRAM-MANIPULATION INSTR
Has calls, jumps, and returns.
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction.
Iteration control of loops.
IV—PROGRAM-STATUS-MANIP INSTR
Zero, sign, overflow, carry, overflow trap, interrupt enable, and sticky bit (records previous value of carry during right shifts).
Can set and clear some bits.

Specification summary: 16-bit µC with split-memory architecture; 8k-byte ROM and 232 bytes of register-file RAM on chip. External memory expandable to 64k bytes, with data bus dynamically programmable as 8 or 16 bits. Register-to-register architecture with ALU operating directly on register file. Has 8-channel, 10-bit A/D converter; four 16-bit software timers; PWM output; five 8-bit I/O ports; full-duplex serial port; and high-speed pulse I/O ports. At 12-MHz clock frequency, 16-bit addition takes 1 µsec, 16×16-bit multiply or 32/16-bit divide takes 6.5 µsec. Average instruction-execution time is 1 to 2 µsec. New CMOS parts have twice the performance of NMOS. In 48-pin DIP, 68-pin PLCC, or 68-pin PGA.

HARDWARE — SUPPORT — SOFTWARE

From Intel: Development kit ($2695) includes iSBE-96 emulator board and ASM-96 macroassembler and runs on IBM PC host as well as Intellec Series III and IV. Real-time emulation to 12 MHz. VLSICE-96 advanced emulator provides real-time emulation as fast as 12 MHz and is hosted on IBM PC as well as Intellec Series III and IV. Intel also offers support hardware for the 80C196 chip.
Programming support for EPROM versions supplied through Intel's line of universal PROM programmers as well as third-party programmers from companies such as Data I/O, Stag, and Elan.

From Intel: Macroassembler (ASM-96), PL/M-96, and C-96 compilers. PL/M and C compilers supply hardware-control features such as interrupts. Each software package includes relocation/linkage utility (RL-96); library management utility (LIB-96); object-to-hex conversion utility (OH-96); and FPAL-96, a 32-bit floating-point utility. Software packages run on IBM PCs and compatible computers. $750 for a single-user license.
From Archimedes (San Francisco, CA): ANSI C-8096 compiler with additional features, such as control of interrupt. Hosted on IBM PC ($995), MicroVAX ($3995), and VAX ($5995).
From Cybernetic Micro Systems (San Gregorio, CA): Graphics programming and simulation aids, which run on IBM PCs ($295 and $995, respectively).

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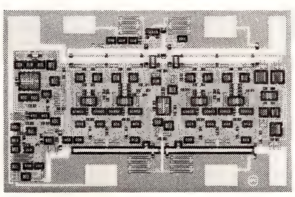

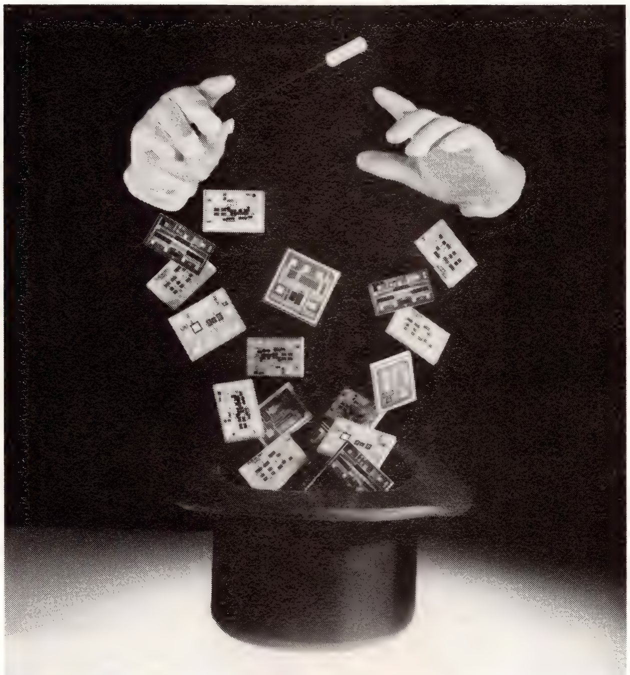

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- 30 dB gain control range
- Gains as high as 26 dB
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The IFD-series low phase noise static prescalers offer:

- Divide-by-4 to 5 GHz
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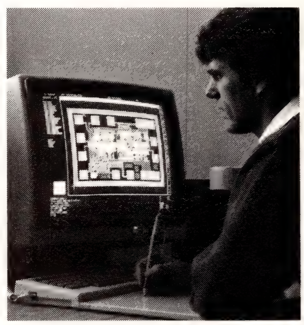
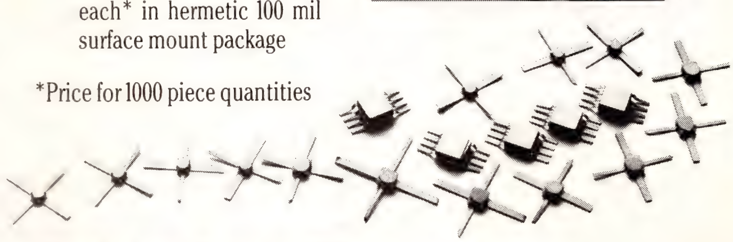




Magic Solutions in Silicon

AVANTEK

CIRCLE NO 186

HPC16000

16-BIT CMOS

AVAILABILITY: Now for 20- and 30-MHz parts.
COST: Less than $5 in volume.
SECOND SOURCE: None.
CORE: The HPC family is core based. National says the family of standard parts is continuously growing. National offers a configurable controller approach based on a library of microcontroller building blocks.

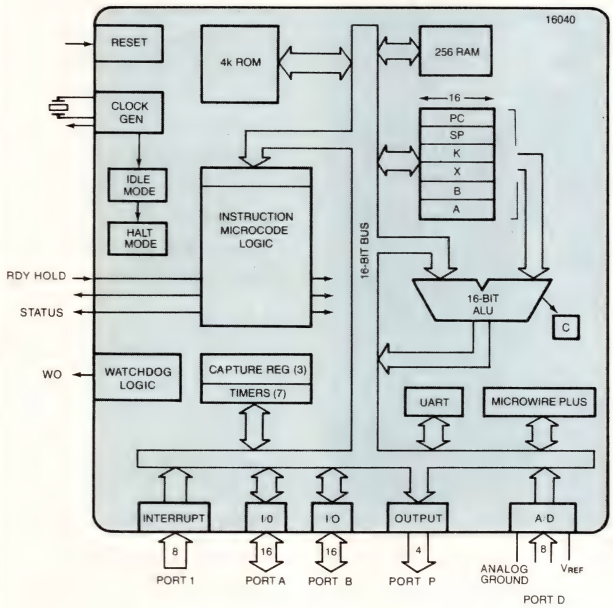
Description: 16-bit CMOS microcontroller family with basic version having 8k bytes of onboard ROM, 256 bytes of RAM, extensive I/O, and onboard peripherals. Original 16040 had 16.8-MHz clock with 240-nsec register instruction execution. Due to shrinking, new HPC16083 is offered in both 20-MHz and 30-MHz versions. The 30-MHz part's shortest instructions are just 134 nsec over −55 to +125°C.

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000

For more information, Circle No. 455

Status: Supplier says HPC16040 and 16083 are first members of what is to be a family of industrial controllers. Supplier's benchmarks (August '86 with HPC at 17 MHz) indicate that HPCs outperform other similar 8- and 16-bit controllers such as Intel 8051 and 8096, Motorola 68HC11, and TI370 on both throughput and ROM-program efficiency. NEC 78XXX and Zilog Super Z8 weren't mentioned. Some Dataquest numbers show the HPC as the largest selling 16-bit CMOS microcontroller. This family is from the same group at National that has produced National's most successful µP/µC, the 4-bit COPS.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Family is designed around common µP core for instruction-set consistency, with various models having various assortments of on-chip peripheral functions. Onboard peripheral functions planned are ADCs, gate arrays for customization, dual-port RAMs for efficient interprocessor communication (download/uploading), and EEPROMs.
2. Microwire/Plus is used for synchronous serial data communications with supplier's Microwire peripherals (ADCs, display drivers, EEPROM), COPS 4-bit µCs, 8050 8-bit µCs, and other HPCs for multiprocessing.
3. Watchdog logic monitors operations and signals upon the occurrence of any illegal activity, such as infinite loops.
4. Halt and idle modes provide additional power savings by stopping clock or disconnecting it.
5. Emulator parts are available for the HPC family.
6. µPI (Universal Peripheral Interface) port for connecting to µPs such as National's 32000 family.

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit arithmetic in binary, including multiply and divide with 32-bit results.
Logical AND, OR, XOR, and compares.
Bit manipulation of all registers and through all 64k address space.
II—DATA-MOVEMENT INSTRUCTIONS
10 addressing modes: register B indirect, register X indirect, direct, indirect, indexed, immediate, register indirect with autoincrement/decrement, register indirect with autoincrement, and skip.
Instructions include load, store, push, pop, and exchange.
III—PROGRAM-MANIPULATION INSTR
Calls, jumps, returns, and conditional jumps implementing high-level-type constructs.
IV—PROGRAM-STATUS-MANIP INSTR
There is a carry bit and several status registers. They may be manipulated as all bits in register space, and in 64k address space, they may be set, reset, and tested.

Specification summary: 16-bit CMOS µC and µP with memory-mapped architecture and 8k-byte ROM and 256-byte RAM on chip. External memory expandable to 544 bytes or more. 16-bit-wide architecture includes data bus, ALU, and registers. Has eight programmable 16-bit timers, eight vectored interrupts, full-duplex UART with programmable baud rate, PWM outputs, 10 timer-synchronous outputs, four input-capture registers, 52 general-purpose I/O lines. Performance of 16083 at 20 MHz is 200 nsec for register operations and 6 µsec for 16×16 multiply and 32/16 divide. Performance of 16083 at 30 MHz is 134 nsec. Supplier says its "microCMOS" process will consume 47 mA at 20 MHz. Idle instruction will reduce this to 1 mA, and halt instruction will drop it to 200 µA. Supply range is 4 to 5.5V. Available in industrial (−40 to +85°C) and extended (−55 to +125°C) temperature ranges (MIL-STD-883 now). In 68-pin PLCC, LCC, 68-pin PGA, and 84-pin TapePak.

COMMERCIAL VERSION (0 TO 70°C)	INDUSTRIAL VERSION (−40 TO +85°C)	MIL VERSION (−55 TO +125°C)	ROM EPROM (BYTES)	RAM (BYTES)	I/O PINS	TIMER BASE COUNTERS	OTHER
HPC46003	HPC36003	HPC16003	ROMLESS	256	52	8	4 INPUT CAPTURE REGISTERS
HPC46004	HPC36004	HPC16004	ROMLESS	512	52	8	4 INPUT CAPTURE REGISTERS
HPC46064	HPC36064	HPC16064	16.0k	512	52	8	4 INPUT CAPTURE REGISTERS
HPC46083	HPC36083	HPC16083	8.0k	256	52	8	4 INPUT CAPTURE REGISTERS
HPC46104	HPC36104	HPC16104	ROMLESS	512	52	8	4 INPUT CAPTURE REGISTERS AND 8-CHANNEL ADC
HPC46164	HPC36164	HPC16164	16.0k	512	52	8	4 INPUT CAPTURE REGISTERS AND 8-CHANNEL ADC
HPC46400	HPC36400	HPC16400	N/A	256	56	4	HDLC & DMA
HPC46400*	HPC36400E	HPC16400E	N/A	256	56	4	HDLC & DMA
HPC467164*	HPC367164	HPC167164	16.0k	512	52	8	EPROM & ONE-TIME-PROGRAM-MABLE DEVICE
HPC46083MH			8.0k	256	52	8	EPROM

*AVAILABLE IN 1990
ALL DEVICES HAVE 8 INTERRUPTS, IMPLEMENT THEIR STACKS IN RAM, HAVE AT LEAST 1 SERIAL I/O PORT, AND COME IN 68-PIN PACKAGES.

HARDWARE — SUPPORT — SOFTWARE

A designer's kit is available for less than $500. Supplier's HPC Development System costs approximately $7000 for the HPC family. A high-end development system will be available from Hewlett-Packard as part of the HPC64700 in 1990. Both development systems can be used in conjunction with various hosts like IBM PCs, PC/XTs, PC/ATs, VAXes, or HP9000 Series 300s.

Cross-assembler and C compiler to run on IBM PC. VAX (Unix/VMS) support is available, as is a symbolic debugger. Floating-point math and general math packages are currently available. Extensive application software is available for ISDN and SCSI.
Dial-A-Helper is a 24-hr on-line computer bulletin board serviced by National. It provides latest information on all National µC chips (including development systems) and also specific application support. Call (408) 739-5582 for more information.

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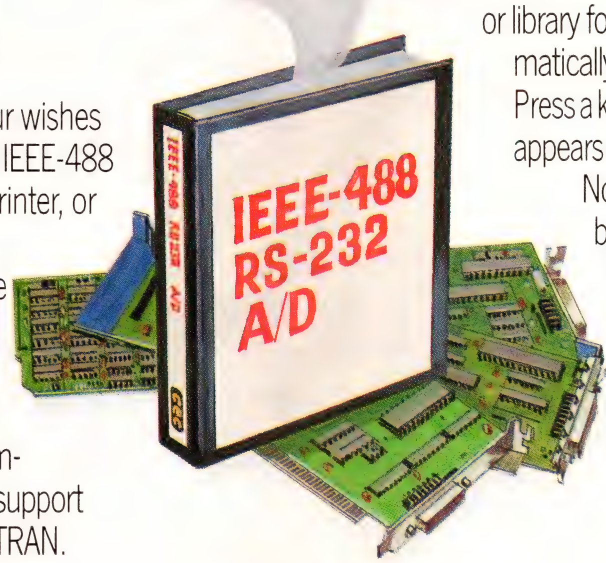

If your wish is for a custom program, CEC also offers software that writes '488 programs. Simply pop up our software over your program editor and select a control function or library for your instrument. Code is automatically generated from your choices. Press a key and the magic begins. The code appears where you want it in your program.

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cec

Capital Equipment Corp.
99 South Bedford Street
Burlington, MA 01803
Tel: 617-273-1818 Fax: 617-273-9057

CIRCLE NO 74

RTX 2000 16-BIT CMOS

AVAILABILITY: The RTX 2000-8 (8 MHz), the RTX 2000-10 (10 MHz), and the RTX 2001A-8 and -10 are available now in 84-pin PGA and PLCC packages.
COST: In 100-piece quantities: 8-MHz RTX 2000 starts at $136; the 10-MHz version starts at $179; the 8-MHz RTX 2001A starts at $57; the 10-MHz RTX 2001A starts at $89.
SECOND SOURCE: Zoran Corp (Santa Clara, CA).
CORE: Available in the Harris Advanced Standard Cell and Compiler library.

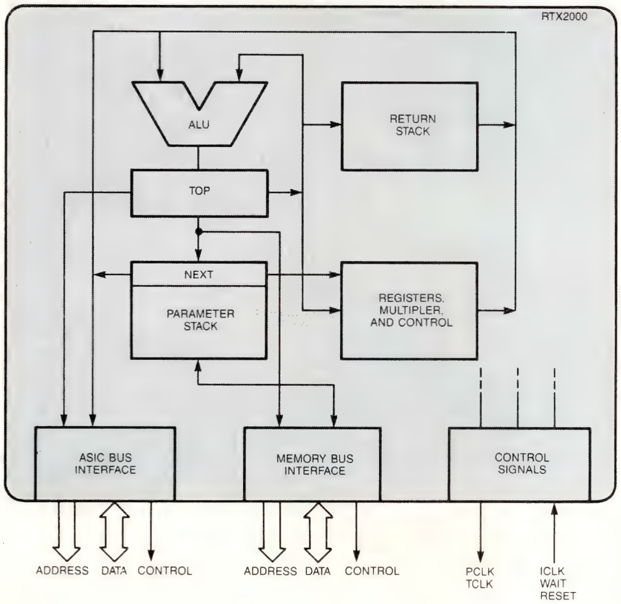
Harris Semiconductor
Box 883
Melbourne, FL 32902
Phone (407) 724-7418

For more information, Circle No. 456

Description: The RTX 2000 is a high-performance 16-bit µP with on-chip timers, interrupt controller, multiplier, and two 256-word stacks. The manufacturer claims that the chip offers a sustained performance greater than 10 MIPS, because each instruction requires only one clock cycle for execution. The chip's architecture lets designers add hardware accelerators and I/O devices that extend the chip's basic structure. The CMOS RTX 2000 operates between dc and the maximum clock rate. Power consumption is typically 5 mA/MHz.

Status: Although Harris places its RTX 2000 in a RISC microcontroller category, the chip fits into the general-purpose µP category, too. The company expects that most of the chip's applications will fall into the real-time embedded-control realm. Because the chip directly executes Forth-language commands, Harris expects that designers will find it relatively easy to do real-time software development. Harris designed the RTX 2000 using its advanced standard-cell and compiler library. Thus, designers can incorporate the device into ASIC chips.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram shows basic RTX 2000 architecture. The 2001A is a smaller version that lacks the hardware multiplier.
2. The ASIC-bus interface lets designers extend the chip's basic architecture with peripheral and I/O devices.

I—DATA-MANIPULATION INSTRUCTIONS
Full set of math and logic instructions, which includes a single-cycle 16×16-bit multiplication operation as well as division and square-root operations. The architecture also allows 16- and 32-bit shifts. You can directly manipulate the top element of either the return or the parameter stack.
II—DATA-MOVEMENT INSTRUCTIONS
Access memory as bytes or words.
Memory-to-stack or stack-to-memory operations require two cycles.
Combine memory or I/O operations with ALU operations.
Access memory in LSB-MSB or MSB-LSB order.
"Streamed" memory access with automatic address update.
Access to 1M byte of memory space through page register.
III—PROGRAM-MANIPULATION INSTR
Intrapage calls require one cycle; interpage calls take three cycles.
Return operations require either zero or one cycle.
Single cycle conditional or unconditional branch operations. Conditional branches depend on the top-of-stack or on the index registers.
Single-level software interrupt.
IV—PROGRAM-STATUS-MANIP INSTR
Flags include interrupt enable, interrupt pending, carry, complex carry, byte order, and boot.
Automatic interrupt enable on return-from-interrupt operation.

Software notes:
1. The RTX 2000 directly executes Forth-language statements—there is no assembly language.
2. Harris claims that the stack architecture is flexible enough that the chip can efficiently run many popular computer languages. The chip contains a parameter and a return stack.

Specification summary: 16-bit CPU with 1M-byte address space. Bus cycles execute in 100 nsec with a 10-MHz clock. All instructions execute in 1 or 2 cycles, and the memory bus is active during every cycle. Additional I/O bus for high-speed transfer operations occurs simultaneously with memory-access and processing operations. The architecture includes two 64-word stacks, both of which may be active when memory- and I/O-transfer operations take place. Harris claims a peak data-transfer rate of 80M bytes/sec. On-chip peripheral devices include 3 counter/timer units and a 16-bit multiplier. The 107,000 mil^2 RTX 2000 or 80,000 mil^2 RTX 2001A come housed in an 84-pin PGA or an 84-pin PLCC package.

HARDWARE — SUPPORT — SOFTWARE

From Harris: A Real-Time Express Development System (10 MHz, TRXDS-10; $2995) runs from within an IBM PC or compatible. Harris also offers 8- and 10-MHz development boards (from $1495) for those who want to write their own development software.
From others: The MicroProcessor Engineering (Southampton, UK; US agency is AMICS Enterprises, Rochester, NY) Power Board is a stand-alone unit that furnishes a variety of I/O ports and 500k bytes of RAM. VME Inc (Milpitas, CA) offers VMEbus development systems and stand-alone boards based on the RTX. Future Inc (Blacksburg, VA) sells IBM PC/PS2 and Apple Macintosh development environments for the RTX.

From Harris: Available software includes a target/host monitor; a PC-based Forth development system; an RTX Forth cross-compiler; a disassembler; and a DOS file utility program. A Forth kernel and a multitasking operating system are available.
From others: Laboratory Microsystems (Marina del Rey, CA), Forth Inc (Manhattan Beach, CA), and others have software packages for the RTX 2000 µP. MicroProcessor Engineering's Power Forth for its development board is an extended Forth-83 development environment.

T222, T425, T800 TRANSPUTER — 16/32-BIT CMOS

AVAILABILITY: Now for 20- and 25-MHz parts; 30-MHz devices are planned for 1990.
COST: In 100 quantities: T222, $57; T425, $146; T800, $348.
SECOND SOURCE: None, but with Inmos's recent acquisition by SGS-Thomson, a second fabrication plant in Carrollton, TX, has been committed to Transputer production.

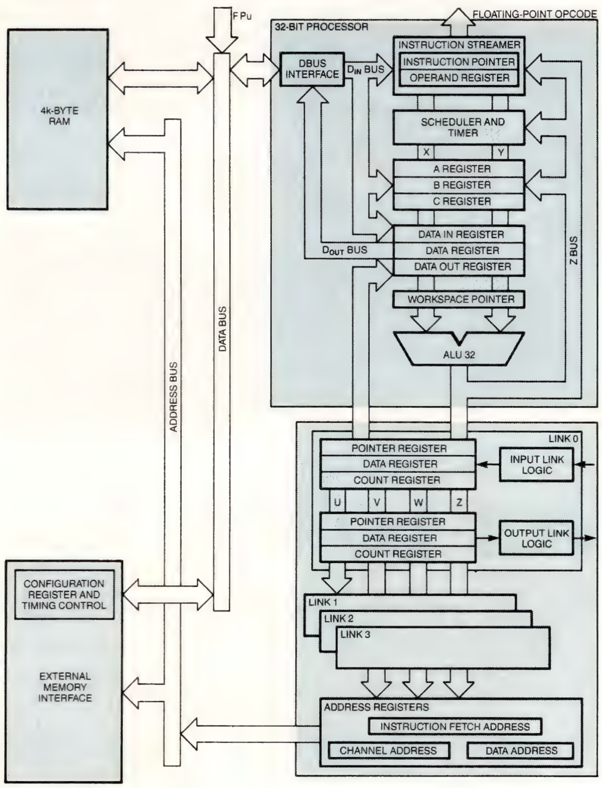
Description: The Transputer family is a range of 16/32-bit μPs. Each member is fully software compatible and conforms to the same basic architecture. The Transputer has both RISC and CISC features; there is a microcode ROM, but a number of commonly used instructions execute in one cycle. Each Transputer has a CPU, 4k bytes of on-chip single-access static RAM, 4 serial links, timers, and an external memory bus. T8XX variants have an on-chip, 64-bit floating-point unit. The Transputers can communicate through their serial links, with no external logic, to other Transputers, suggesting multiprocessor-system applications. The serial links are DMA channels into the Transputer memory system and allow software processes to run on independent Transputers and communicate directly via the links.

Inmos Corp
Box 16000
Colorado Springs, CO 80935
Phone (719) 630-4000

For more information, Circle No 457

Status: Volume buildup has been slow. One possible explanation is that most of the applications have been for multiprocesssor configurations (typically 4 to 10 Transputers), so designers have been engrossed by the challenge of developing practical parallelism. There are now over 1000 designs worldwide using the Transputer, and the new owner, SGS-Thomson, is expanding production capabilities with a second manufacturing plant in the US.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Integer arithmetic, including multiply and divide. Logicals, shifts, and comparisons. T800 has on-chip IEEE floating-point add and subtract, multiply and divide, and square root, both 32 and 64 bits.

II—DATA-MOVEMENT INSTRUCTIONS
Memory-bandwidth block moves, 2-dimensional block moves for graphics BitBlt. Load/store of local variables done relative to workspace pointer. Indexed load/stores available from address in A register. Immediate loads done 4 bits at a time. Large immediate values loadable from tables, instruction stream, or a sequence of special instructions.

III—PROGRAM-MANIPULATION INSTR
Conditional and unconditional jumps. Procedure call and return. Subroutine call and return. Computed jumps. Process (task) creation and deletion. 2-level priority and time-sliced scheduling with message passing and time events, using built-in hardware. One level of interrupt.

IV—PROGRAM-STATUS-MANIP INSTR
Error flag detects overflow. Test, set, clear, stop-on-error instructions. One error flag per task priority level. Instructions for checking array bounds.

Software notes:
1. Frugal 4-bit operation code allows only 16 basic instructions. Most of these are movement types (category II) involving one workspace-pointer-relative 4-bit address and used to push and pop data on and off evaluation stack.
2. Two priority-ordered process queues are each supported by front and back registers, indicating a linked list of processes ready to run. Event-based multitasking is fully supported by a real-time kernel in microcode.
3. Supplier's Occam language said to facilitate programming multiple Transputer systems, but programmer must still study how best to partition task. Third parties have announced extensions to C to accomplish same ends.

Hardware notes:
1. Diagram is for T425. T800 is the same but adds an FPU. T801 is the same as the T800 except that the external memory interface is a nonmultiplexed data/address bus instead of the T800 multiplexed bus. T222 is the same as the T800 except that it has a 16-bit internal architecture and the floating-point unit has been removed.
2. Unlike most 32-bit machines, there's no group of general-purpose registers. Instead, substantial on-chip RAM plays equivalent role.
3. ALU fed from 3 accumulators forming a small 3-deep stack, allowing compact implied addressing.
4. The four serial links allow arrays of Transputers in multiprocessing with no bus saturation, which is why speed increase is said to be linear when more μPs are added.

Specification summary: Family of 16- and 32-bit μPs designed for multiprocessing. Unique in that they have the hardware and software links that allow them to be hooked to each other for parallel processing. Four full-duplex, 20M-bps serial links driven by on-chip, 8-channel DMA provide basic multiprocessor communication links as well as I/O. One 5-MHz external clock generates 20-MHz chip clocks, giving 50-nsec instruction cycle. Submicrosecond interrupt latency, procedure call, and task switch. Most instructions take 1 or 2 cycles. Integer multiply takes 38 cycles, and divide takes 39 cycles (under 2 μsec). Single-precision floating-point add takes 7 cycles (350 nsec), floating-point multiply takes 11 to 18 cycles (550 to 900 nsec), and floating-point divide takes 16 to 28 cycles (800 to 1400 nsec).

HARDWARE — SUPPORT — SOFTWARE

T800, T414, and T212 are available as discrete components in a variety of packages including PGA, PLCC, and ceramic quad flatpack. Speed options are 17, 20, and 25 MHz. 30 MHz is planned for '90. Multiprocessor boards are built by simply plugging the required modules. Each module has a standard 16-pin interface with the 4 serial links, power, grid, reset, and analyze pins available. Inmos provides mother boards for PC, VME, and Eurocard environments; third parties support host systems such as Macintosh, PS/2, and Q-Bus for MicroVax. Modules are supplied by Inmos and third parties, for example, IMS B411 with IMS T800 and 1M-byte dynamic RAM, or IMS B404 with 2M-bytes dynamic RAM and 32k bytes static RAM. Application modules such as Ethernet and graphics modules are also available.

Inmos supplies compilers for standard hosts such as the IBM PC, VAX(VMS), and Sun. These compilers include a parallel Kernigan and Ritchie C compiler, a parallel Fortran compiler to ANSI X3.9-1978, an Occam compiler, and a Pascal compiler to ISO 7185 and BSI 6192 1982. Third parties supply a range of other compilers including Ada, Modula 2, and Prolog as well as C and Fortran compilers.

The Third Vision

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Brüel & Kjær

89-088

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Z8000/Z80000 — 16/32-BIT NMOS AND CMOS

AVAILABILITY: Now for NMOS Z8000 at 4, 6, 10, and 12 MHz. Now for NMOS Z80000 at 8 and 10 MHz. CMOS version for Z8000 is called 16C00. CMOS for Z80000 will be available in '90.
COST: $9.96 for Z8000 (10k) in PLCC package.
SECOND SOURCE: AMD (licensed), SGS-Thomson, and Sharp for Z8000. NEC for Z80000, by mask exchange.
CORE: Zilog has both Z8000 and Z80000 as cores in its "in-house" ASIC library, planning to use Zbus for its systems on silicon. Says that 160 × 160-mil Z8000 core is small enough to leave room for other functions on practical 400 × 400-mil ASIC chip.

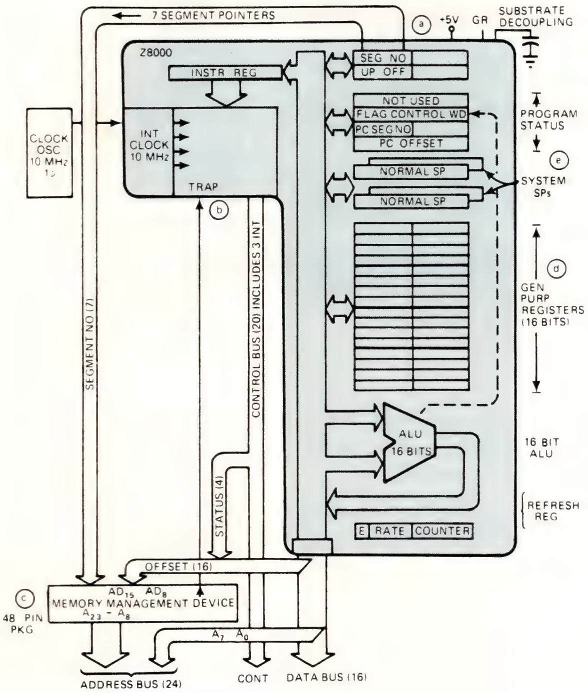
Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000

For more information, Circle No. 458

Description: One of first μPs to have architectural features of a modern minicomputer. Original 16-bit Z8000 comes in 40-pin package for addressing 64k-byte memory or in 48-pin package for addressing 8M-byte memory. Said by many industry observers to be architecturally more powerful than 8086 but less powerful than 68000. Supplier says military has found it to be highest performance 16-bit μP, offering best CPU speed, interrupt handling, and character-string search. 32-bit version, Z80000, is superminicomputer-like enhancement that remains object-code compatible with the Z8000. Has cache for data and instructions and an MMU.

Status: The Z8000 has found most acceptance in real-time control applications, particularly military, according to Zilog. The company has added the Z16C00 16-bit CMOS microcomputer to the family for real-time embedded control applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
Supplier has companion peripherals suitable for both processors:
For Z8000, a range of DMA, FIFO, data ciphering (NBS), communications, and counter/timer parts.
For Z80000, two 32-bit parts: a Z32104 CMOS DMA controller, which contains 32-bit address and data buses with 8-bit peripheral bus; and a Z32106 CMOS floating-point coprocessor that implements IEEE P754 format.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including add, subtract, decimal adjust, increment, decrement, multiply (signed), divide (signed).
Logicals, including AND, OR, exclusive OR, compare, test, complement, rotate, and shift (by n).
Operations can be on bit, BCD nibble, byte, 16-bit word, or 32-bit double word, and can use any of the 16 general-purpose registers as accumulator.
The Z32106 floating-point processor will do IEEE-754 operations.
II—DATA-MOVEMENT INSTRUCTIONS
Eight addressing modes using general-purpose registers as indexers and stack pointers.
Comprehensive set of block-transfer and string-manipulation macroequivalents, including many dedicated to I/O space.
III—PROGRAM-MANIPULATION INSTR
Call and call relative (± 4096 bytes).
System call using special system stack pointer.
Jump conditionals.
IV—PROGRAM-STATUS-MANIP INSTR
Set and reset flags, complement flags. Set-multiple-interrupt modes.
Tests for the micro-in and micro-out lines for multiple-microprocessor configurations.
V—SYSTEM-CONTROL INSTRUCTIONS
The 80000 has privileged instruction for exclusive use by an operating system.

Specification summary: Common-memory architecture with optional separate I/O space and separate "systems" stack. Z8000 is 16-bit μP that has directly addressable memory space of 8M bytes (8001, 8003) using segment pointers, expandable to 48M bytes using the six available memory spaces and an MMU. Executes 110 basic instructions with 410 combinations at speeds ranging from 0.30 μsec through 1 or 2 μsec to 7 μsec for 16-bit multiply, all at 10-MHz system clock (4 and 6 MHz also available). Eight large-computer-style addressing modes. NMOS, requiring one 5V supply (plus substrate-decoupling capacitor), in either 40- or 48-pin package. Z80000 is a 32-bit upwardly compatible version of Z8000 and can run same software. 6-stage pipelining of instruction fetch/execute cycle and 256-byte on-chip associative cache for instructions and data for improved performance (and use of 100- to 120-nsec memories). Also on-chip MMU for virtual memory with address bus a full 32 bits for 4G-byte memory space. At 25-MHz, clock has 12.5-MHz (80-nsec) instruction cycles that give 12.5-MIPS burst rate (when doing loops out of cache) and 5 MIPS continuously (4 MIPS with MMU virtual-memory translation). 16 × 16 multiply in 1.2 μsec and 32 × 32 in 1.9 μsec. 2-μm NMOS dissipates 3 to 4W. Initial samples have been packaged in ceramic PGAs, but lower-cost Z80320 will have muxed address and data buses and be in 68-pin PLCC.

HARDWARE — SUPPORT — SOFTWARE

From Zilog: Z-Scan 8000 in-circuit emulator ($5500). 500-pg Z8000 technical manual.
From others: Applied Micro, Boston Systems, Hewlett-Packard, Kontron, Orion, Single Board Solutions, Sweet Micro System, and Tektronix. Contact supplier for addresses.

From Zilog: Real-time application software (PC-based). C and PLZ/SYS compilers.
From others: Real-time executive from Ready Systems (Palo Alto, CA), VRTX/8002 ($5775), which is suited to embedded applications, and an Ada compiler ($795) from Meridian Software Systems (Laguna Hills, CA). Contact supplier for names and addresses of others.

1750A

16/32-BIT CMOS

AVAILABILITY: Now from Allied-Signal Microelectronics Center, LSI Logic, and United Technologies Microelectronics Center (UTMC).
COST: Allied-Signal charges $760 (1000) for its part screened to 883C level B. The LSI Logic part costs $900 (100). The full 883C part from UTMC, to Standard Military drawings (SMD), costs $704 (100), and for full military temperature and high-reliability screening, the part is $624.
SECOND SOURCE: In negotiation.

Description: MIL-STD-1750A defines an instruction set architecture for airborne computers. The standard leaves the implementation to the discretion of the chip vendors. The 1750A standard was developed to allow the use and re-use of available software support, such as compilers and instruction-level simulators. Radiation-hardened versions of many of the 1750A implementations are available.

Allied-Signal
Microelectronics Center
9140 Old Annapolis Rd
MD 108
Columbia, MD 21045
Phone (301) 964-4047

For more information,
Circle No. 737

LSI Logic
1501 McCarthy Blvd
Milpitas, CA 95035
Phone (408) 433-7557

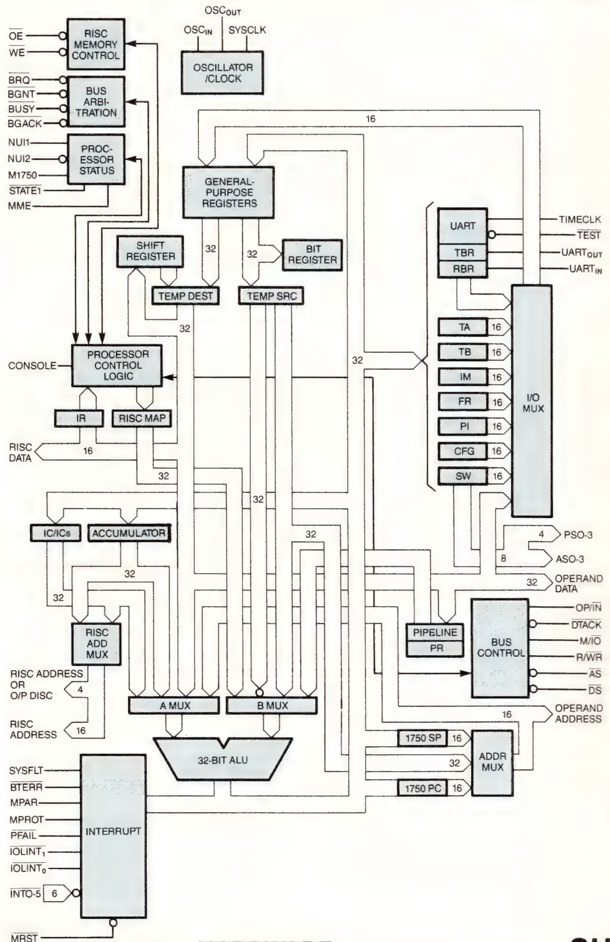
For more information,
Circle No. 738

United Technologies
Microelectronics Center (UTMC)
1575 Garden of the Gods Rd
Colorado Springs, CO 80907
Phone (800) 645-8862

For more information,
Circle No. 739

Status: The Allied-Signal 40-MHz device has been in production for 2 years. A 50-MHz version will extend performance to 6.0 MIPS on the integer DAIS (Digital Avionics Instruction Set) mix and to 4.1 MIPS on full DAIS with floating point. The Allied-Signal MMU chip and LSI Logic's 1750A processor are also in production. UTMC's unit is in full production as an 883C product to the Defense Electronics Supply Center (DESC) standard military drawing. UTMC offers the device to 10^5 total dose radiation hardness to data-sheet specifications.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS

Add, subtract, multiply, divide, and compare. Logicals and shifts. The instructions also provide bit-manipulation capabilities such as set, reset, and test. Single- and double-precision fixed floating-point and extended floating-point formats.

II—DATA-MOVEMENT INSTRUCTIONS

Instructions let you move data from register to memory, memory to register, between registers, and to the stack. Loads and stores in all formats plus test and set-bit operations.

III—PROGRAM-MANIPULATION INSTR

Conditional and unconditional jumps and branches. Calls are also supported. Stack management instructions suitable for high-level languages. Handles 16 levels of prioritized interrupts.

IV—PROGRAM-STATUS-MANIP INSTR

Emulation-mode status register accessible through input/output instructions. Instructions for accessing status, interrupt mask, and fault registers.

Specification summary: The Allied-Signal version is a single-chip implementation that includes timers, counters, a hardware multiply and a floating-point unit. The LSI Logic L64500 1750A implementation has a 16-bit CPU, which is expandable to 32 bits, depending on the operation. Like the other 1750As, the L64500 uses separate address and data buses to enhance system performance. You can augment the LSI Logic device with the L64550 to implement optional enhancements to the MIL-STD-1750A. The L64550 includes an MMU with memory-expansion capabilities to 1M words, a block protect unit, a memory fault status register, a bus arbitration unit with six bus masters, the start-up ROM interface, an I/O port, a trigger-go counter, and other options.

Hardware notes:
Diagram is for the UTMC 1750AR. The unit functions as a stand-alone RISC processor providing 8 MIPS at 16 MHz. In the 1750A operation mode, a throughput of 750 kIPS (thousand instructions/sec) at 12 MHz is achieved using the DAIS mix. The basic µP accepts 64k bytes of memory, which you can expand to 1M byte by using an MMU. The chip supports the 1750A console mode.

HARDWARE — SUPPORT — SOFTWARE

UTMC provides application information for customer-fabricated VME boards. You can use a PC with the software tools to provide interactive simulation and debugging of system configurations.
Allied-Signal Microelectronics Center offers a development system for the A-S BX1750A that converts an IBM PC into a real-time, mappable monitor/debugger. An Ada source-level interface is under development.
Mikros Systems (Mercerville, NJ) has a single-board computer with debug monitor, 64k bytes of RAM, and two RS-232C console interfaces. Call UTMC for contact phone numbers.
Tasco (Bellevue, WA) has an ICE pod for the HP 64000 development system. Call LSI Logic for contact phone numbers.

Assemblers and compilers are available from several outside sources. Mikros Systems offers high-level debug software for their single-board computer/IBM PC system.
UTMC offers a software package to aid in the development and debugging of system software and hardware. The software tool kit consists of a RISC Monitor or 1750 Monitor, along with an interactive RISC simulator.

340X0 GRAPHICS μP FAMILY — 32-BIT CMOS

AVAILABILITY: Now for 34010 and 34020. The 34082 floating-point unit is in early sampling.
COST: The 34010 costs $40 (10k); the 34020 costs $110 (10k); and the 34082 floating-point unit costs about twice as much as the 34020 for samples.
SECOND SOURCE: Under active consideration.

Texas Instruments Inc
MOS Microcomputers
Box 1443, MS736
Houston, TX 77001
Phone (713) 274-2340

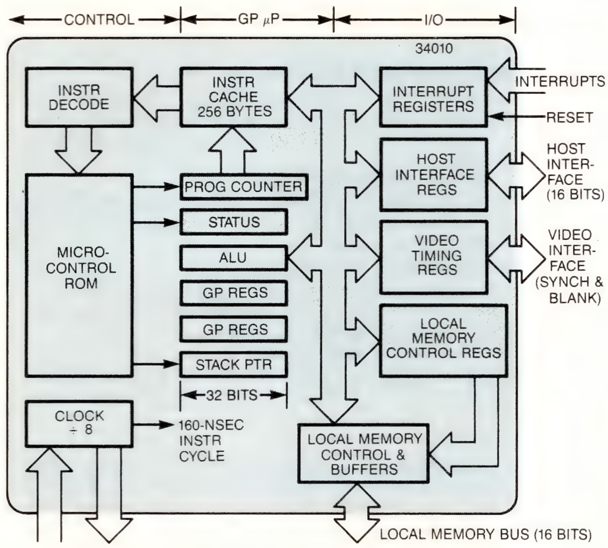
For more information, Circle No. 740

Description: This 32-bit CMOS μP family is optimized for graphics-display systems. But because it has true general-purpose Von Neumann architecture, it can be used for other applications that need the same bit manipulations that are required in pixel manipulations of CRT-type raster graphics. Features built-in instruction cache and ability to simultaneously access memory and registers. In addition to regular μP instructions, it has specialized instructions for pixel manipulation. 1G-byte address space is bit addressable on bit boundaries using variable-width data fields (1 to 32 bits). The 34010 has a multiplexed external 16-bit address/data bus, whereas the 34020 is a full 32-bit machine. The 34020 has additional enhancements including more graphics-specific instructions, but it is also upwardly object-code compatible with the 34010.

Status: This μP family is included in the directory despite its obviously specialized slant toward CRT graphics because it has a general-purpose Von Neumann architecture and instruction set. Also, some of its attributes can be equally applied to other, nongraphics applications. In particular, the μP is included because of its ability to do rapid bit manipulation of a large local address field. From the number of IBM PC-based board-level products that incorporate this part, it can be concluded that it is a success. One nongraphic area being explored by users is industrial control, where bit manipulation and low cost relative to other 32-bit μPs is attractive, according to TI (even for consumer-oriented uses such as arcade games). In some cases, designers in nongraphic areas are making clever use of some special graphics features. TI began sampling the 34020 in March '89. Volume production is planned for the first qtr '90.

CHARACTERISTICS

HARDWARE



Hardware notes:
1. Diagram represents 34010.
2. Added graphics features are embodied in the second 16×(32) register file and among 28 16-bit I/O control registers. They allow programmable pixel and pixel-array processing for both monochrome and color systems of variable pixel sizes. Hardware incorporates 2-operand raster operations with Boolean and arithmetic operations, x-y addressing, window clipping, window "pick" operations, 1-to-n bits/pixel transforms, transparency, and plane masking.

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
General-purpose μP instructions: add and subtract, multiply and divide, rotate and shift, compare and logicals.
Special graphics instructions: add, subtract, and comparisons relating to x-y coordinates.
II—DATA-MOVEMENT INSTRUCTIONS
General purpose: Move byte, move field, move register.
Special graphics instructions: Move x half of register, move y half of register, pixel transfer, pixel block transfer.
III—PROGRAM-MANIPULATION INSTR
Call subroutine, conditional decrement and skip, push/pop, software interrupt, return from interrupt.
IV—PROGRAM STATUS-MANIP INSTR
Has 32-bit status register (not all bits used) that can be accessed and used for program-manipulation decisions.

Specification summary: 32-bit general-purpose CMOS processor with added hardware and software features to support CRT raster graphics. Chip contains two 16×(32) register files, hardware stack pointer, and 256-byte instruction cache. One of the 16-word register files contains stack pointer and 15 general-purpose registers (the equivalent of the general-purpose registers found in regular nonspecialized μPs). Addressing modes of these registers are tuned to support high-level languages. Other register file is dedicated to CRT control as described in hardware note. Has 32-bit-wide address-data bus to support a gigabyte of off-chip "local" memory space. Interfaces directly to dynamic RAMs and video RAMs (including dual-port RAMs). A microcoded local memory controller supports pipelined memory write operations of variable-size fields that may be executed in parallel with ALU operations. Has separate 16-bit-wide data bus and associated control pins to interface with host μP. Fabricated in 5V CMOS and packaged in 68-pin PLCC. The new chip is compatible with the 34010, but provides a 512-byte cache and supports 1M-bit video-RAM chips.

SUPPORT

HARDWARE

From TI: TMS34010 software development board ($1495), which plugs into IBM PC or compatible. Used for evaluation, familiarization, and software development, and comes with user interface and debugger software. TMS34010 XDS/22 emulator box ($14,995) operates as a stand-alone unit with nonintelligent terminal or with IBM PC or compatible as host. The TMS34020 Software Development Board and Hardware Emulator System will be introduced first qtr '90.
From others: Board-level and other hardware support now available from numerous sources. See TI's *TMS 34010 3rd-Party Guide* (call (800) 232-3200, ext 701, and ask for literature No. SPVB066B).

SOFTWARE

From TI: TMS34010 assembler package ($500) for IBM PC and compatibles using MS-DOS 2.11 or higher and for VAX ($1000) using VMS, Unix Berkeley 4.2, or Unix System V. Includes macroassembler/linker, source/object-code archiver, and ROM utility. MS-DOS version also has a 34010 simulator.
Texas Instruments has developed TIGA-340, a standard software interface for the TMS340 family of graphics processors. Development tools for TIGA (Texas Instruments Graphics Architecture) include a $340 Driver Developer's Kit that helps software developers make their existing software run on TIGA-compatible 34010 boards; a $1500 Software Developer's Kit for those who want to develop direct 34010 code or custom downloadable extensions to TIGA, which includes a 34010 C compiler, an assembler, bit-map font and math/graphics source-code libraries, and a $15,000 software porting kit for hardware developers to make their 34010-based systems TIGA compatible.
From others: Software now available from numerous third-party sources such as JMI (Spring House, PA), which has developed a real-time executive. See the TI TMS 34010 3rd-Party Guide mentioned under Hardware Support.

Text continued on pg 169

68000 FAMILY

8/32-BIT, 16/32-BIT, 32/32-BIT NMOS AND CMOS

AVAILABILITY: Now for all models to 33-MHz 68020. Samples of 68030 are available to 50 MHz. The 68040 has been announced but is delayed. The original design used NMOS technology, and CMOS versions are designated by 68HCXXX, however all designs since the 68020 were only made in CMOS and don't use the HC identifier.
COST: In 100 qty, prices range from less than $10 for low-end 68008 and 68000 to $500 for 50-MHz 68030.
SECOND SOURCE: Rockwell, Hitachi, SGS-Thomson, and Signetics/Philips all licensed with mask interchange for 16-bit parts. Motorola says it plans to keep 68020 and 68030 to itself for the time being.
CORE: Motorola has plans to use members of the 680x0 family as cores around which it'll build application-specific processors to address specific markets.

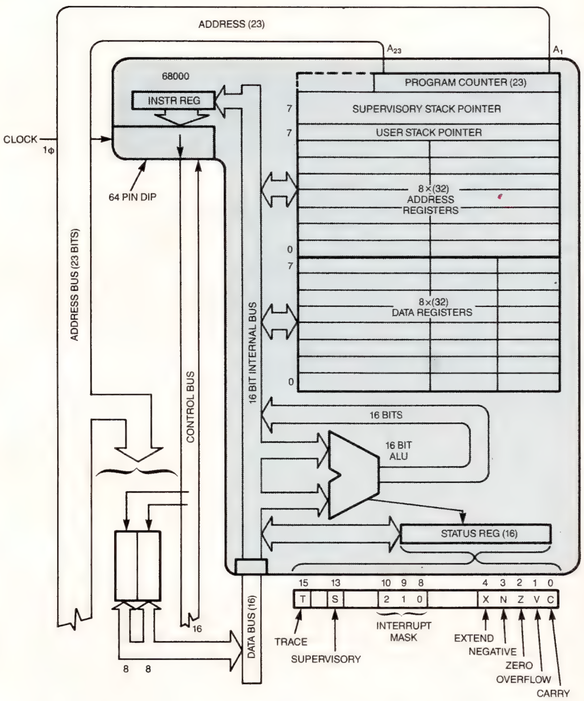
Description: Family based on a modern minicomputer architecture using a basic group of 16 fairly general, 32-bit registers. The 68008 has a narrow 8-bit data bus. The 68000 has a midsized 16-bit data bus and ALU, and 24-bit addressing. The 68030 is full 32 bits throughout with instruction and data caches and MMU on board.

Motorola Integrated Circuits Div
3501 Ed Bluestein Blvd
Austin, TX 78721
Phone (512) 928-6000

For more information, Circle No. 741

Status: Part of the success of the 68000 family is due to the success of the Apple Macintosh II, and much of the rest is due to 68020 and 68030's popularity among builders of Unix-based workstations. The 68030 is similar to the 68020 but with an extra cache for data (in addition to the 68020 instruction cache) and with the 68851 MMU on board. The 68040 is a full 68000-compatible µP containing an IU (integer unit), an FPU (floating-point unit), an MMU (memory-management unit), and instruction and data caches. The 680x0 family has received considerable competition from the RISC µPs, including Motorola's own 88000 RISC chips.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram favors the basic 68000, which although it has 32-bit-wide registers, has 16-bit-wide ALU and data buses and only 23-bit-wide address bus. It comes in 64-pin DIP, 68-pin PGA, and 68-pin PLCC.
2. Bottom-of-the-line 68008 has only 8-bit data bus and 20- or 22-bit address bus. It comes in 48-pin DIP and 52-pin PLCC.
3. Upper-range 68010 is similar to 68000 but supports virtual memory. 68010 has 24-bit address bus and comes in a 64-pin DIP, 68-pin grid array, or 68-pin PLCC.
4. Top-of-the-line 68020 and 68030 are full 32 bits throughout, including ALU and address and data paths. Both have instruction caches, and the 68030 also has a data cache and an MMU. The 68040 adds an FPU.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including multiply and divide (signed and unsigned).
Logicals and rotates and shifts.
Can handle bits, BCD nibbles, bytes, short (16 bits) and long (32 bits) words.
(Floating-point coprocessors 68881/2 available.)
II—DATA-MOVEMENT INSTRUCTIONS
Five basic address modes are register direct, register indirect, immediate, absolute, and program-counter relative. To these modes can be added postincrementing, predecrementing, offsetting, and indexing.
Can use eight 32-bit address registers as indexes or stack pointers. The eight 32-bit data registers can also serve as indexes.
III—PROGRAM-MANIPULATION INSTR
Branch and jump to subroutine. Branch conditionally.
Link and unlink instructions invoking one address register as frame pointer (used to establish temporary local environments in structured programming).
Seven levels of priority interrupts, including nonmaskable, with 256 possible interrupt vectors.
IV—PROGRAM-STATUS-MANIP INSTR
16-bit status register is software accessible.
Sophisticated trap operations help user debug programs.
Trace mode.
V—SYSTEM-CONTROL INSTRUCTIONS
Privileged instructions for operating systems and multiprocessor communication.

Specification summary: 68020: full 32-bit CPU version of the 68000 family that's object-code compatible with all members. Has 16 32-bit general-purpose data and address registers, 32-bit ALU with barrel shifter, and 32-bit data bus. Also has full 32-bit address bus that can reach 4G bytes of direct linear external memory. Supports instruction-continuation-type virtual memory. Has 256-byte instruction cache on chip and 3-stage pipelining. At 25-MHz maximum clock, executes 5 MIPS. For tight inner loops with so few instructions that they can be contained in cache, and when data can be contained in registers, the 68020 will operate at burst modes to 12 MIPS. With 68881, it can run at 1.25M Whetstones. Has 18 addressing modes and instructions to support structured high-level languages and sophisticated operating systems. Fabricated in 1.5-µm CMOS with 1.5W power dissipation. Packaged in 114-pin grid array. 68030 is similar to 68020 but also has data cache and incorporates a subset of the 68851 MMU. It will run at 30 to 50 MHz and have 2× 68020 performance at systems level. It is fabricated in 1.2-µm CMOS (with planned shrinkage to 1.1 µm). Packaged in 128-pin grid array.

HARDWARE — SUPPORT — SOFTWARE

HDS-300 hardware/software development station ($15k to $20k) provides real-time emulation of 68000 family µPs with bus-state-analyzer support and source-level debugging. MEX68KECB educational computer board is based on 68000. VM04 is a 68020-based 32-bit Versamodule interconnected within a target system using the 32-bit, asynchronous, Versabus interconnect standard. VME130 is a 68020-based, 32-bit VME bus module using Eurocard mechanical format.
From third parties: Family is widely supported by makers of universal µP development systems. Also, the VMEbus system architecture is used in a broad range of applications with more than 150 independent suppliers of compatible products.

VersaDOS real-time operating system, system V/68 operating system, CP/M-68K operating system, concurrent DOS-68K operating system, and VRTX real-time operating system ($6775 from Hunter Systems). Unix support from Motorola includes direct ports of Unix V, AT&T. X assembler for Exormacs and VME/10, X-C compiler VME/10, and Exormacs for VAX/780 are available.
From third parties: Supplier has catalog listing the outside support for family. New type of support is software to allow 68000 to run MS-DOS (8086) programs: by emulation from Phoenix (Norwood, MA) and by Insignia (London, UK, but with offices in San Francisco); and by binary translation from Hunter Systems (Palo Alto, CA).

SERIES 32000

8/32-BIT, 16/32-BIT, 32/32-BIT NMOS AND CMOS

AVAILABILITY: Now for all older NMOS and some CMOS replacements for NMOS parts. The new CMOS 32532 is available now.
COST: From \$1 to \$975 (100) (see table).
SECOND SOURCE: None.
CORE: National is using the 32000 as the basis for its application-specific embedded processors.

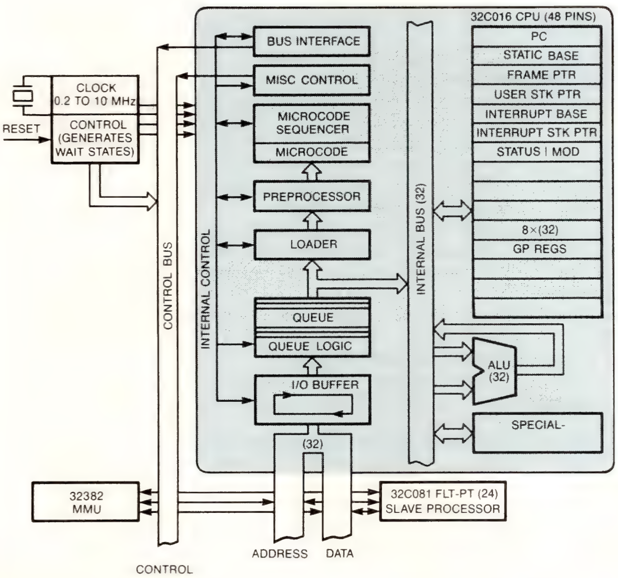
National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000

For more information, Circle No. 742

Description: A 32-bit µP family in which various models bring out different-sized address and data buses. The fully 32-bit core processor has acquired a reputation, even among competitors, for being "elegant" in its symmetry; that is, its instructions and addressing apply regularly to all registers, which supplier claims makes high-level-language compilers easier to write. It also has reputation for needing less memory space for programs. These software virtues should apply to all family members as strict code compatibility is maintained across line. Family is intended to match the needs of operating systems like Unix and to have big-computer features expected of 32-bit systems, such as demand-paged virtual memory, protection of operating system from users, and protection of one user from another user.

Status: National says that because all its 32XXX family members are full 32-bit internally, those members with 8- and 32-bit external data buses should also be included, which would bring the total up to 700,000 units or roughly on par with what Motorola and Intel are claiming for their 68020 and 80386. What seems critical now is how well the new 32532 is received. It appears to be a good CISC machine, and if it can run at the promised 30 MHz and deliver the promised 10-MIPS sustained performance, it should be attractive for use in multiprocessor Unix systems (whether in reprogrammable or embedded applications).

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
All instructions operate on either 8-, 16-, or 32-bit data and can be accessed by any appropriate addressing mode. Multiply and divide, BCD arithmetic, logicals and bit manipulation throughout memory space and CPU registers.
II—DATA-MOVEMENT INSTRUCTIONS
Intelligent string operations and bit-field handling allow efficient movements.
III—PROGRAM-MANIPULATION INSTR
Stack- and frame-pointer instructions suitable for high-level languages (including Polish notation). Modular software support via special CPU hardware (Mod register) and tables automatically implemented for indirect addressing of position-independent ROMs, etc. Array instructions.
IV—PROGRAM-STATUS-MANIP INSTR
Status registers in slave processors and MMU as well as in CPU, with both privileged and user access.

Hardware notes:
1. Floating-point chip (NS32580) is example of slave-type processors that National is using to extend CPU. These processors will be integrated on CPU when VLSI processing technology permits; they are transparent to programmer and recognize op codes not used by CPU.
2. Advanced features include demand-paged virtual memory, position-independent ROM code and multiprocessing. Latest 32532 has instruction and data caching sufficiently sophisticated to handle multiple-processor situations. Supplier claims relaxed memory-access specifications, even at 30 MHz.

Specification summary: 32-bit "maxi-mini"-type pipelined architecture implemented in multichip NMOS VLSI. Uniform addressing of up to 4G memory locations. Instruction set chosen to match operations needed by high-level-language compilers. All instructions can symmetrically apply to all data types (8, 16, and 32 bits, etc) and all register and memory locations. Performance of family ranges from ¾ to 10 MIPS (sustained). The top-of-line Model 32532, when running at maximum 30-MHz clock, has a peak performance of 15 MIPS and a Dhrystone benchmark of 16.3k. It has 4-stage overlapping execution pipeline that includes instruction prefetch and branch prediction. It has parallel address and data units, each with own buses and 32-bit ALU. Separate caches for instruction and data: the instruction cache is 1k bytes (direct mapped); the data cache is 1k bytes, 2-way set associative. On-chip demand-paged virtual MMU with 64-entry associative translation look-aside buffer. Fabricated in 1.5-µm double-metal CMOS. Packages range from 48-pin DIP for 32008 to 175-pin grid array for 32532. LCC and PLCC packages available for some models.

HARDWARE — SUPPORT — SOFTWARE

From National: SYS32/20 that converts IBM PC/ XT and PC/AT into a Series 32000 development tool (from \$3500). Splice in-system emulation covers family µPs up to 32332 with support for 32532 on way. Development/evaluation boards based on 32016, 32032, and 32332 are also available from National and from other suppliers (contact National for list) with prices from \$532 to \$9900.
From others: PC plug-in board with 32016 or 32032 and memory (\$2000 to \$3000) that allows running Unix from Opus Systems (Cupertino, CA). PC-based logic-analysis workstation by Northwest Instrument Systems (Beaverton, OR).

From National: Series 32000 Software Catalog is guide to available software from third-party vendors. It lists compilers for C, Pascal, Fortran, Cobol, Modula-2, Ada, etc. Supplier says its GNX (Genix Native and Cross) languages and tools and its optimizing compilers can increase performance and code density as much as 2×. Operating systems include supplier's Genix V.3.1 derived from AT&T System V, release 3.1.
From others: Software-analysis workstation from Northwest Instrument Systems (Beaverton, OR). Software coprocessor from Phoenix Technologies (Norwood, MA) that allows family to run MS-DOS 8086 programs. VRTX real-time multitasking operating system from Ready Systems (Palo Alto, CA) and MTOS-UX from Industrial Programming Inc (Jericho, NY).

VL 86C0X0 ARM

32-BIT CMOS

AVAILABILITY: Now for production volumes of 86C010. 86C020 samples available now, production fourth qtr '89.
COST: $45 for 86C010 in volume; $145 (100) for 86C020.
SECOND SOURCE: Sanyo Semiconductor Ltd sources the 86C010.
CORE: Part of VLSI's cell library. (Was designed by customer Acorn Computers using VLSI's semicustom tools.)

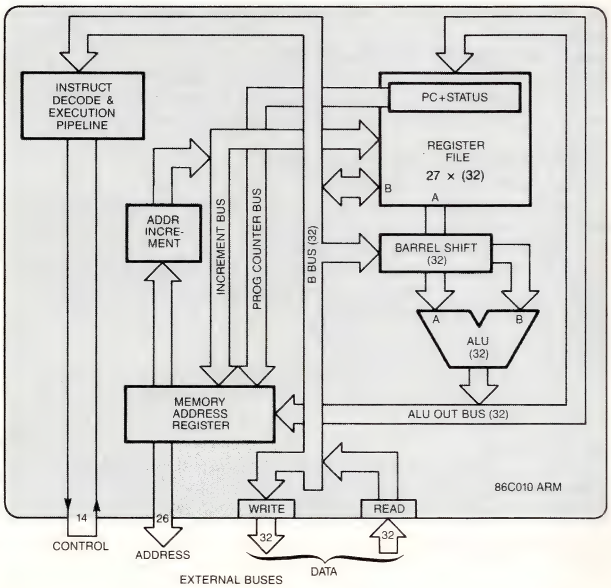
VLSI Technology Inc
8375 S River Pkwy
Tempe, AZ 85274
Phone (602) 752-8574

For more information, Circle No. 459

Description: ARM stands for Acorn-RISC machine (RISC stands for reduced-instruction-set computer). The VL86C020 is software compatible to the '010. The second-generation chip includes a 4k byte, unified instruction and data cache on chip. The cache uses 64-way set-associative replacement with random replacement to provide a 93% hit rate. Current devices operate at 20 MHz with 35-MHz operation available by year end as the µP migrates into a 1.0-µm process technology. Low power consumption of ½W suggests the part for embedded-controller applications.

Status: VLSI is currently sampling the VL86C010. The company supplies evaluation boards, assemblers, and C compilers directly. The architecture of the chip is targeted at the embedded-controller market and provides performance similar to most competing RISC processors at lower cost. VLSI wants to sell the VL86C020 for less than $55 in high-volume production. The low cost is further enhanced because the cost of the cache memory is included in the processor price. Cost is kept low because of small die size (approximately 280 mils square in a 1.0-µm process) and 160-pin plastic quad flatpack packaging. A dedicated coprocessor bus necessitates the high pin count. The 86C020 has found application in laser printers, network controllers, disk controllers, and graphics subsystems.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, logicals, and comparisons. Bit clear. Shifts (barrel shifter with ALU).
II—DATA-MOVEMENT INSTRUCTIONS
Most data movements are by register-to-register instructions with option for multiple-register addressing. Only load and store operations to memory (typical of RISC). The VL86C010 includes a semaphore operation to support multiprocessing applications.
III—PROGRAM-MANIPULATION INSTR
Skip-type decision instructions (though old-fashioned, this simple approach can give fastest response in some cases). Branch instruction has option where combined PC and status register are copied in R14 data register for quick, simple return.
IV—PROGRAM-STATUS-MANIP INSTR
Usual status bits are combined with PC and mode-control bits in a 32-bit-long register. This allows all three elements to be saved in one fell swoop.

Software notes:
1. Only 44 instructions, in keeping with RISC concept.
2. Simple RISC instructions are said to ease the task of writing efficient high-level-language compilers.
3. User and supervisory modes with supervisory mode being entered by software interrupt.

Hardware notes:
1. In addition to 86C010 µP, VLSI has associated set of chips for memory (86C110), video (86C310), and I/O (86V410). For floating-point math, VLSI suggests using one of the commercially available coprocessors such as AT&T's WE32206.
2. Note the 27 registers. This is less than on some RISC machines, but they do overlap as is common in RISC to speed interrupt service (overlapping gives automatic saving of data). This means programmer only sees 16 registers at most, and of these, only 15 are general purpose.
3. Some provisions for memory management, including cache and virtual memory through abort-signal, mode-control bits.

Specification summary: 32-bit CMOS Von Neumann (common memory) µP with RISC-style architecture. Has simple ALU with associated barrel shifter and set of 32 registers on CPU µP chip, 16 of which are accessible to programmer. Has some features expected in a large-memory-space machine: instructions and controls to handle virtual memory and caching. 32-bit external data bus and 26-bit external address bus allow linear addressing for external 64M-byte memory space (can be addressed on 8-bit-byte or 32-bit-word basis). Only simple load and store instructions for external memory. 10- to 12-MHz, 2-phase clock gives 4- to 5-MIPS sustained performance with 10 to 12 MIPS max. Interrupt latency is 2.75 µsec max. No provisions for separate I/O addressing so I/O must be memory mapped. Fabricated in 2-µm CMOS with chip 230 mils on side. 0 to 70°C temperature range. Packaged in 88-pin JEDEC Type-B leadless ceramic chip carrier and plastic leadless chip carrier.

HARDWARE — SUPPORT — SOFTWARE

VLSI says that much of the hardware support comes from Acorn. There is a PC-form-factor board ($2500) for software development. (Note: It can be expected that VLSI will bias its support toward the ASIC approach, in which the ARM µP will be considered a core around which the customer will be encouraged to apply "application-specific" I/O, memory, etc; thus, VLSI's ASIC design tools might be considered part of the hardware support.)

VLSI indicates that most of the software support comes from Acorn. There is an assembler for the ARM's instruction set, a Basic interpreter, and compilers for popular high-level languages (C and Fortran-77). There are also compilers for artificial-intelligence languages (Cambridge Lisp and Prolog). Typical pricing for software is $500 each.

AVAILABILITY: 16, 20, 25, and 33 MHz in production (at 4 locations). 80386SX, 80376 samples available now.
COST: In 1000 qty, $189 for 16-MHz 80386, $201 for 20-MHz 80386, $249 for 25-MHz 80386, $319 for 33-MHz 80386, $80 for 16-MHz 80386SX, and $53.10 for 16-MHz 80376.
SECOND SOURCE: None announced or planned in immediate future.

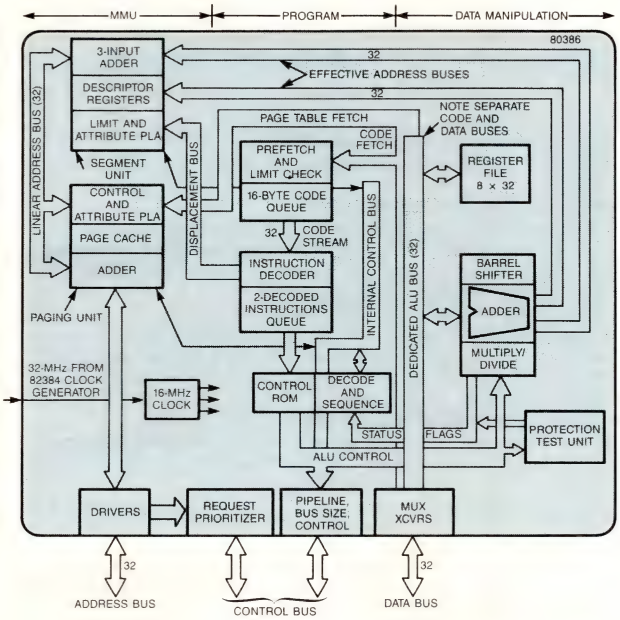
Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

For more information, Circle No. 460

Description: The 32-bit 386 family of μPs is compatible with the 8086 and 80286 families. Included are address translation registers and a 32-bit address bus for up to 4G bytes of physical memory and 64T bytes of virtual memory (the SX and 376 processors only have a 24-bit address bus). Runs DOS, Windows, OS/2, Unix, iRMX, and iRMK. Virtual 8086 mode allows direct execution of 8086 software under new 32-bit operating systems. The 386SX permits the manufacture of less-expensive systems with full 386 software capability.

Status: All things point to the 80386 remaining the dominant 32-bit μP, certainly for the next 5 years. The 386 is the sole μP carrying the IBM PC momentum into the 32-bit world. Not satisfied that it "owns" the MS-DOS and OS/2 world, Intel is now aggressively after the Unix world and is in production with the 80376—a version of the 386 aimed at the embedded-controller world. Intel also offers the 80386SX, another version of the 386 that supplies a 16-bit data bus and a 24-bit address bus.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. No on-chip cache, but 33-MHz 82385 cache controller ($114.66 for 33 MHz (1k)) for implementing 32k-byte external cache.
2. On-chip MMU chip said to allow for memory management with no penalty in bus bandwidth (if off chip, supplier says, an extra cycle would be needed). Allows choices of segmentation or paging singly or in combination for multiuser protection and for virtual memory.
3. The 80386 has its own math coprocessor, the 80387, which costs $406.85 for 33 MHz, $99.75 for 25 MHz (1000).
4. Along with the 80387 and 82385, the 80386 can use the 82380 32-bit peripheral combination chip that incorporates DMA and interrupt support and interval timers, etc.
5. The 80376 is compatible with the 386 programming model, but cannot run 8086 or real-mode programs. The chip has a 16-bit external bus.

I—DATA-MANIPULATION INSTRUCTIONS
Bit manipulation and bit-string manipulation (aided by 64-bit barrel shifter).
Conversion between bytes, words, and double words.
Arithmetic, including 16-bit and 32-bit operands and 32-bit signed and unsigned multiply and divide.
(80387 math coprocessor has full IEEE-754 instructions, including all transcendentals.)
II—DATA-MOVEMENT INSTRUCTIONS
String moves and gang push and gang pop of all registers.
Instructions to insert and extract bit strings (additional addressing modes for existing instructions allow more flexibility in assignment of registers).
III—PROGRAM-MANIPULATION INSTR
Repeat instructions based on flags.
Enter and leave procedure instructions, conditional or unconditional branch to anywhere in 4G-byte memory space.
IV—PROGRAM-STATUS-MANIP INSTR
Flag instructions mostly same as on 8086 (contains 4 debug registers, allowing breakpoints on data or code accesses, even when in ROM).
V—HLL AND OS INSTRUCTIONS
Instructions for checking array bounds.
Segment assignment instructions.
Load and store descriptor tables for protection (processor context switch via 1 instruction).

Software notes:
1. Only those instructions beyond basic 8086 instructions described.
2. 80386 said to be object-code compatible with previous members of 8086 family and can run their operating systems. There is a "virtual 8086" mode in which 8086 (and 8088) code can be run within the protected 386 environment.

Specification summary: A more or less standard, "classical" 32-bit minicomputer architecture that has a basic register set similar to the previous 16-bit members of 8086 family so that it can directly run their machine code. It has added features that make it more general and suited to larger 32-bit environments: data-manipulation instructions that can be applied to almost any register, high-level-language-oriented instructions, operating-system-oriented instructions, and on-chip MMU. Fabricated in 1.5-μm CMOS (supplier calls it CHMOS-III), it's expected to consume no more than 400 mA at 32-MHz external clock (16 MHz internal). Packaged in 132-lead ceramic PGA.

HARDWARE — SUPPORT — SOFTWARE

ICE-38625D in-circuit emulator ($22,495) supports 386DX μP to 25 MHz and ICE38633D supports to 33 MHz. ICE386SX in-circuit emulator ($19,495) supports 386SX to 20 MHz. ICE376D in-circuit emulator ($18,495) supports 376 to 20 MHz. All Intel ICE in-circuit emulators for the 386 family operate on a common emulator base. They provide control and display software with a common Intel windowed user interface with drop-down menus and source code display hosted on DOS on PC and PS/2 systems. The iPAT Performance Analysis Tool provides a real and protected mode software analysis with high-level access to target-system performance analysis and test-case coverage in real time for target systems based on the 386 family at clock speeds to 20 MHz. An iPAT-386 probe supports the 386DX μP. You can also interface the iPAT-386 to the probes of ICE in-circuit emulators for the 386DX, SX, and 376 μPs. Various Multibus I and II single-board computers are also available from Intel and other vendors for the 386DX μP.

From Intel: ASM-386 macroassembler ($600), RLL-386 binder and system software builder utilities ($600), and the MON-386 serially hosted debug monitor ($995). The C-386, Fortran-386, and PL/M-386 compilers (each $900) support 386 μP family protected-mode software cross-development on DOS hosts. VAX/VMS kit support including ASM, RLL, compilers of choice, and VMS DB-386 incorporating a 386 system software simulator is also available on MicroVAX ($14,000) and VAX ($18,000) systems for cross-development.
From others: Rapidly growing third-party support. Most important are MS-DOS and forthcoming OS/2 from Microsoft (Bellevue, WA). (There are variations in DOS such as Concurrent DOS by Digital Research (Monterey, CA.)) Next is Unix V from AT&T (Morristown, NJ) and Zenix from Microsoft. Also real-time executives from Ready Systems (Palo Alto, CA), JMI Software (Spring House, PA), and others. In addition there are dual combinations of operating systems such as Unix-DOS, CTOS-DOS, and DOS-DOS.
Note: Some software depends on 386 mode.

80486 FAMILY

32-BIT CMOS

AVAILABILITY: The 25-MHz version will be in production in fourth qtr '89. Samples available now.
COST: The 25-MHz 80486 will cost $950 (1000).
SECOND SOURCE: None announced or planned for immediate future.

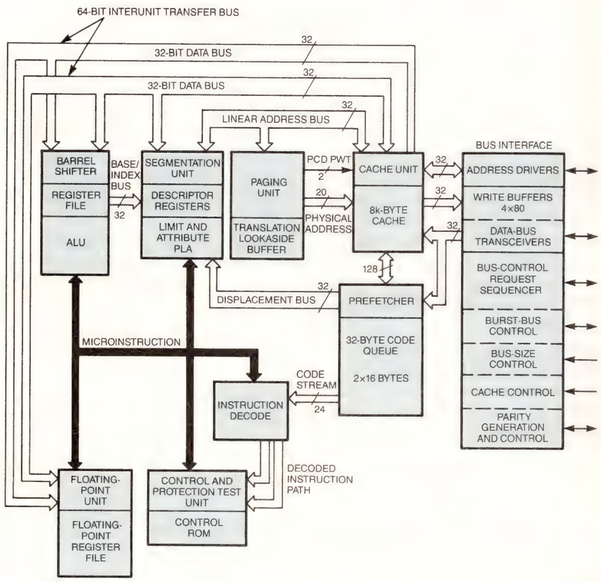
Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

For more information, Circle No 461

Description: The i486 CPU is comprised of an enhanced 80386 CPU, an enhanced 80387 math coprocessor, an 82385 cache controller, an 8k-byte combined code and data cache, and a paging and memory-management unit. The i486 is binary compatible with 386/387 processor software but is 2 to 4× faster due to enhanced execution pipelining and higher integration. The i486 CPU adds several new instructions, which support multiprocessor operating systems. Also added is an instruction for artificial-intelligence programs. A byte-swap instruction allows the i486 CPU to read data in either big-endian or little-endian format. A burst bus allows the i486 to fill the on-chip cache with 16 bytes of data in 5 clock cycles.

Status: 25-MHz samples are available now. Volume production is scheduled to begin in fourth qtr '89. 33-MHz samples will be available this year. Intel claims more than 200 design wins.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Information not provided by manufacturer.
II—DATA-MOVEMENT INSTRUCTIONS
Information not provided by manufacturer.
III—PROGRAM-MANIPULATION INSTR
Information not provided by manufacturer.
IV—PROGRAM-STATUS-MANIP INSTR
Information not provided by manufacturer.
V—HLL AND OS INSTRUCTIONS
Information not provided by manufacturer.

Specification summary: Information not provided by manufacturer.

HARDWARE — SUPPORT — SOFTWARE

ICD48633D in-circuit debugger ($12,500) is a hardware-assisted real-time debug monitor supporting 486 μP to 33 MHz with real-time execution control over prototype 486-based systems. ICD48633D supports execution breakpoints, including cached breaks, control of 486 μP execution, and access to registers and system memory. A standard logic-analyzer interface is provided to support cross-triggering between ICD486 and a high-speed logic analyzer. The ICD48633D in-circuit debugger is hosted on DOS PC and PS/2 systems. Host software uses the common Intel windowed interface model with drop-down menus and source-code display.

From Intel: Intel's i486 assembler, compilers, system utilities, and software debuggers are intended for computer system software development requiring access to the full native-mode architecture models of the 486 μP. ASM macroassembler ($600), RLL binder and system software builder utilities ($600), and C and PL/M compilers (each $900) support 486-family protected-mode software cross-development generating 486 instructions in code developed on DOS hosts. Language kits ($4500) including ASM, RLL, a compiler of choice, and the DB debugger are also available. VAX/VMS kit support including ASM, RLL, and a compiler of choice are available on MicroVAX ($7000) and VAX ($9000) systems for cross-development.

CLIPPER

32-BIT CMOS

AVAILABILITY: Now for 40-MHz C100 and C300. Currently sampling 50-MHz versions.
COST: In 1000 qty: C100 module (33 MHz) with clock, $645; C100 chip set (25 MHz), $305; C300 module (40 MHz), $895; C300 module (50 MHz), $1095; C300 chip set (40 MHz), $655.
SECOND SOURCE: None announced.

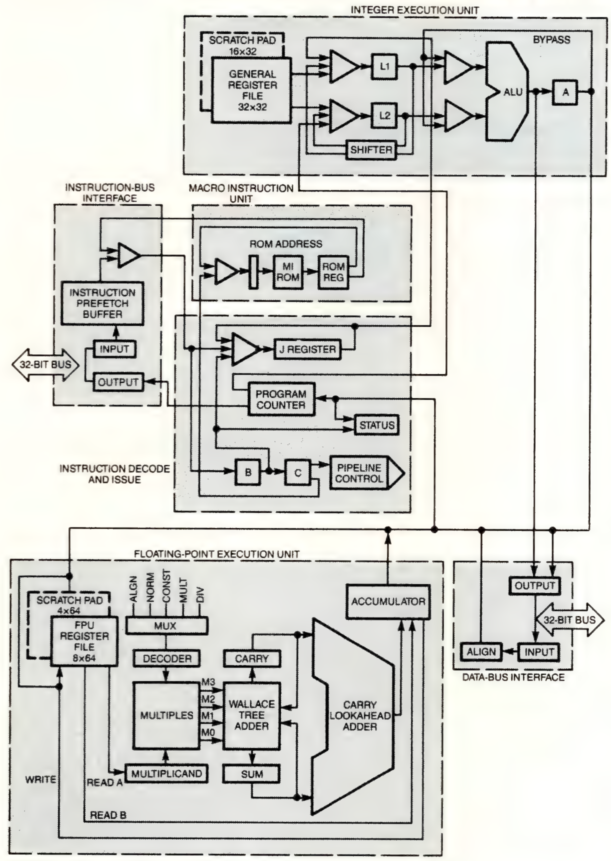
Intergraph Corp
Advanced Processor Div
2400 Geng Rd
Palo Alto, CA 94303
Phone (415) 494-8800

For more information, Circle No. 462

Description: CMOS RISC-based μP has a dual-bus Harvard architecture. 3-chip set includes a CPU that incorporates a floating-point math unit (FPU) and two cache/MMU chips: one for instructions and one for data. Available in first- and second-generation versions in modules, chip sets, and individual chips, the Clipper family can deliver system-level performance ranging from 6 to 20 MIPS.

Status: The Clipper C100 has been in production since early '87; the 40-MHz C300 has been in production since January '89. Over 25,000 units have been shipped through July '89, giving Clipper one of the largest installed bases of any general-purpose commercial RISC processor. The manufacturer claims monthly shipments exceed 1000 units. The C100 is available as a 3-chip set in PGA packages, and the C300 μP is available in production quantities. Future Clippers in both ECL and CMOS are under development; a 70-MIPS ECL version is scheduled for introduction in the first half of '90.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. The CPU chip has RISC-like ALU plus a CISC-like macroinstruction ROM and floating-point unit. The other two chips are identical pin-programmable cache/MMU chips, so one can be used for instruction caching and the other for data caching. The instruction cache carries the CPU's PC (instruction program counter). The 4096-byte capacity of each cache plus the sophisticated caching control (2-way set associative) gives the Clipper a high hit ratio (over 90%).
2. Each cache supports virtual memory via the on-chip MMU. The caches (especially the data cache) operate on a physical memory basis, so less flushing is needed. The C100 requires 135-nsec memory devices, and the C300 requires 90-nsec memory devices.
3. CPU uses sophisticated pipelining with provision for bypassing.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply, and divide (32-bit integer and 32- and 64-bit IEEE floating point done in floating-point unit), floating-point converts, negate, compare, logicals, including AND, OR, EXCL OR, and NOT. 32- and 64-bit shifts and rotates, including floating point.
II—DATA-MOVEMENT INSTRUCTIONS
Architecture favors register-to-register operations and avoids operations on memory other than register-to-memory movements. There are nine addressing modes, including absolute, relative (with and without displacements), relative indexed, and PC (program-counter) indexed. Despite streamlined instruction set, architecture provides efficient string moves, because execution control is switched over to macrocode ROM.
III—PROGRAM-MANIPULATION INSTR
Macrocode ROM is used for context-switching save and restore instructions that support entry and exit from interrupt and trap routines. Push, Pop, supervisor, and user stacks (any register can be used as pointer).
IV—PROGRAM-STATUS-MANIP INSTR
Two status words, a user-program status word, and a privileged system status word (which can only be written in supervisory mode).
V—SPECIAL INSTRUCTIONS
Supervisory mode commands. Hardware supports 18 hardware traps and 128 supervisory calls. Software semiphores are supported for multitasking.

Software notes:
1. Clipper's 168 instructions are a balance between 1-cyle RISC and multicycle CISC commands. The RISC takes care of the simpler, most frequently used instructions. The CISC macrocode takes care of complex instructions such as floating/integer conversion, character-string manipulation, save and restore registers, and trap/interrupt entry and return sequences.
2. C100 and C300 instructions are compatible.

Specification summary: Modified RISC-type architecture in which the basic frugal RISC instruction set is supplemented with boost from microinstruction ROM. The bus-bandwidth bottleneck is solved by having separate buses for instruction and data and putting a cache/MMU chip on each bus. Putting the caches on separate chips allows them to be large enough to generate hit rates over 90%. Partitioning also allows IEEE 64-bit floating point to be incorporated on CPU chip so there is no off-chip delay (as when going to an external coprocessor). There is no need for CPU to have a separate multiply-divide hardware because these operations can be done in the floating-point unit. Performance is 6 to 8 MIPS average for C100 and up to 14 MIPS for C300. For user convenience, the chips are sold mounted with clock on a 3.5×4.5-in. multilayer pc card with 96-pin DIN connector. C100 chips are available separately, too.

HARDWARE — SUPPORT — SOFTWARE

The Clipper Module card integrates the three Clipper chips into a functioning CPU. It provides the clock and PC wiring and a 96-pin DIN connector. User must provide the bus buffers externally. Intergraph supplies development systems that provide a 33-MHz Clipper CPU, 8M bytes of RAM, 156M bytes of hard-disk storage, and an Ethernet interface. Software includes Clix, based on Unix System V; a C compiler, a loader/debugger; and utilities.

Intergraph is firmly committed to software standards. A wide array of standards-based software is available from Intergraph, including Clix V.3.1 (based on Unix V.3.1) operating system; optimizing compilers for C, Fortran, and Pascal; RFS, NFS, and TCP/IP networking software; and X-windows windowing interface. Over 250 third-party packages are available, including compilers for Lisp, Ada, and other languages; tools and utilities; end-user application packages such as Word Perfect, Q-Calc, Q-Office+, Masterplan, and UniPlex II Plus; and the Ingres, Informix, and Oracle database programs.

SPARC RISC

32-BIT CMOS

AVAILABILITY: From Fujitsu: now for MB86901. From Cypress: 7C601 in production now. From BIT: now for ECL BIT SPARC chip set. From LSI Logic: now for 20- and 25-MHz versions of the L64801.
COST: For Fujitsu: $325 (5000). For Cypress: $556 (100). The BIT ECL B5000 Integer Unit alone costs $850; the BIT SPARC chip set costs $3300 for an Integer unit, a floating-point controller, a floating-point multiplier, a floating-point ALU, and two register file chips. For LSI Logic: L64801 (Fujitsu compatible) is $186 (100) in a 179-pin PGA and L64811 (Cypress compatible) is $215 (100).
SECOND SOURCE: Fujitsu, Cypress, and BIT SPARC μPs are different and not hardware compatible. LSI Logic makes two versions—one is Fujitsu compatible and the other is Cypress compatible. But all versions must run SPARC software as defined by Sun Microsystems Inc (Mountain View, CA). Texas Instruments and Philips/Signetics also provide second-sourced μPs.
CORE: Fujitsu has made a start in this direction with a gate array. LSI Logic will also offer RISC elements in its ASIC library.

Description: Goal is to set a high-performance RISC-type software standard while allowing maximum hardware flexibility so that vendors can compete on the basis of performance. Sun Microsystems defined SPARC at instruction-set and programmer's model level and then entered into entirely separate joint agreements with silicon vendors with the intent of reaching 100-MIPS performance by 1990. Meanwhile, Sun provides development hardware and software support via its workstations.

Fujitsu Microelectronics Inc
3330 Scott Blvd
Santa Clara, CA 95054
Phone (408) 727-1700

For more information, Circle No. 408

Cypress Semiconductor
3901 N First St
San Jose, CA 95134
Phone (408) 943-2852

For more information, Circle No. 409

Bipolar Integrated Technology (BIT)
Box 4750
Beaverton, OR 97076
Phone (503) 629-5490

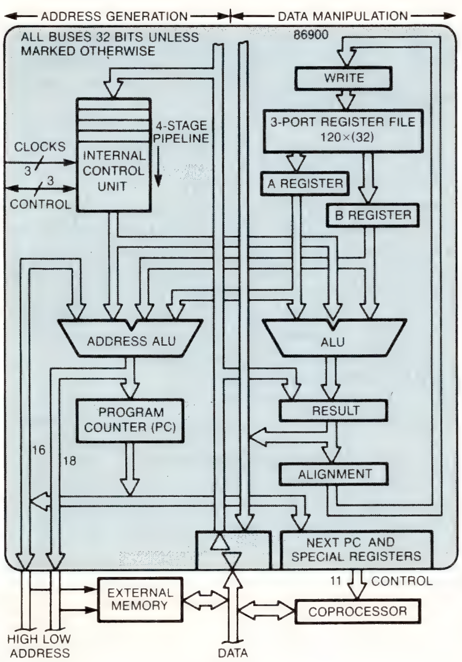
For more information, Circle No. 410

LSI Logic Corp
1551 McCarthy Blvd
Milpitas, CA 95035
Phone (408) 433-8000

For more information, Circle No. 411

Status: Here is another instance where an OEM has developed a μP for its own strategic needs and then let semiconductor vendors openly market the resulting device. A twist in this case is that the OEM, Sun Microsystems, is also a leading workstation vendor and is able to back up the μP with all-important development support. The motivation of all concerned is to demonstrate and promise such dramatic price/performance progress that there's sufficient OEM and third-party following to make SPARC a winner in the current high-MIPS sweepstakes. As with some other RISCs, SPARC lacks full multiply (only multiply step) and thus may need the help of a coprocessor. Currently, over 750 applications run on SPARC hardware. SPARC International (Sunnyvale, CA), a consortium of hardware and software vendors, is dedicated to creating and maintaining open standards and multivendor compatibility of SPARC-based machines and applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram is for Fujitsu 86901. Fujitsu also supplies gate-array companion chip 86910 that provides interface to Weitek 1164/65 floating-point chip set.
2. Cypress will implement its SPARC in full-custom CMOS using Cypress's 0.8-μm 2-layer metal process. The chip set will include an integer unit, a floating-point unit, and cache.
3. BIT has implemented its SPARC in bipolar ECL and will provide companion FPU chips.
4. SPARC stands for Scalable Processor ARChitecture.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply (step). Logicals and shifts.
II—DATA-MOVEMENT INSTRUCTIONS
Load and store to memory (in RISCs, only simple loads and stores used to external memory). Load and store to CPU registers. Load and store to floating-point registers. Load and store to coprocessor registers.
III—PROGRAM-MANIPULATION INSTR
Call subroutine, branch conditional, save and restore, jump and link (there are 128 hardware and 128 software traps, mostly user definable).
IV—PROGRAM-STATUS-MANIP INSTR
Read and write processor state register (note that integer, floating-point, and coprocessor condition codes are mentioned).
V—SYSTEM-LEVEL INSTRUCTIONS
Instruction-cache flush. Can set up system and user modes and associated protection (note that address pins define user and system instruction and data spaces).

Software notes:
1. There are four stages (five in BIT μP) of pipelining, and it is up to optimizing compiler to prevent pipeline breaks by inserting a delay instruction before branch instructions.
2. Overlapped CPU register file windows are said to allow faster context switching than if usual stack were used.

Specification summary: 32-bit μP family that is standardized at software level but open at hardware level. Architecturally, it follows the RISC philosophy of minimum instructions (Fujitsu shows about 107), most of which execute in single cycles (1.3 to 1.7 clocks per instruction). It has a fairly large number of on-chip registers (120) to hold data being processesd for rapid access, which also permits the fixed-length instructions to carry the two source and one destination addresses needed for single-cycle operations (register file has 3-port structure). The on-chip registers are partitioned into seven 24-register groups that are overlapped at edges so that parameters can be easily passed between them. There are also eight global registers. Can address 4G bytes of direct address space and 256 pages of 4G-byte indirect space. Addressing supports various user-defined cache configurations. Fujitsu 86901 has separate coprocessor port that couples tightly to Weitek 1164/65 FP chips. Strategy is to aggressively upgrade performance by frequent redesign in newer technologies as they emerge.

HARDWARE — SUPPORT — SOFTWARE

Sun workstations, even the older models that use Motorola 68000-family μPs, are adequate as Sun maintains software compatibility (obviously the newer models, from Sun-4 onward, which use SPARC, would be ideal). Evaluation boards from Cypress and Fujitsu. Definicon and CAD/CAM International supply development boards. Call Cypress for company phone numbers.

Vendors say they'll pass along Sun's optimizing compilers for C, Pascal, and Fortran as well as Sun's Unix operating system. Wind River Systems (Emeryville, CA) will provide a real-time operating system. A SPARC monitor is available from Bradley Forthware (Sunnyvale, CA).

R2000/R3000

32-BIT CMOS

AVAILABILITY: Now for the IDT and LSI Logic versions; Siemens will have engineering samples in January and full production in the second half of '90.
COST: The IDT 79R3000 is available in volume pricing as low as $80. LSI Logic's LR2000 costs $190 (100), and its LR3000 costs $299 (100). Siemens SAB R2000A and SAB R3000A cost $250 and $350, respectively.
SECOND SOURCE: NEC and Performance Semiconductor.

Integrated Device Technology
3236 Scott Blvd
Santa Clara, CA 95052
Phone (408) 492-8684

For more information,
Circle No. 412

LSI Logic Corp
1551 McCarthy Blvd
Milpitas, CA 95035
Phone (408) 433-7447

For more information,
Circle No. 413

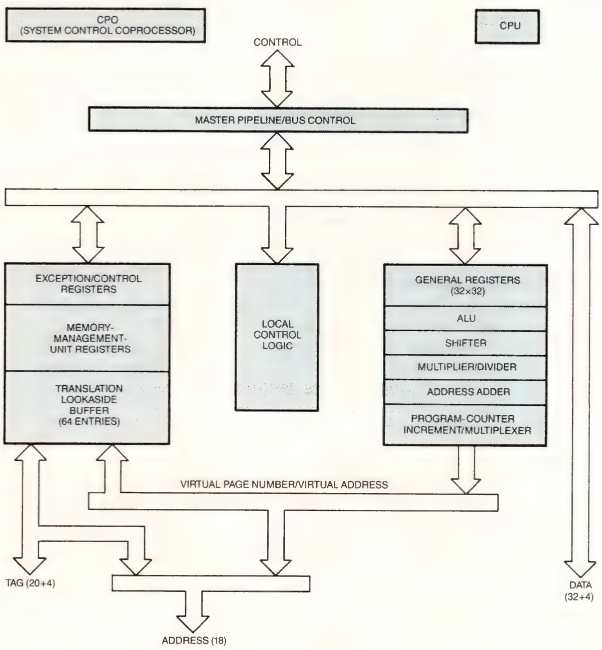
Siemens Components Inc
2191 Laurelwood Rd
Santa Clara, CA 95054
Phone (408) 980-4500

For more information,
Circle No. 414

Description: This reduced-instruction-set-computer architecture was initially developed at Stanford University under the auspices of DARPA (Defense Advanced Research Projects Agency). The original design emphasized concurrent compiler and operating system development. The architecture supports as many as three tightly coupled processors.

Status: The R2000 and R3000 are multisourced, specification-compatible RISC μPs. The architecture has won a number of high-profile designs recently. Such workstation companies as Digital Equipment, Silicon Graphics, Sony, and MIPS have selected the architecture as the one to build their RISC-based hardware on. The R3000 was selected by JIAWG (Joint Internal Avionics Working Group) as a standard for military avionics programs such as the Advanced Tactical Fighter. The range of applications being based on the R2000 and R3000 therefore includes workstations, flight control systems, laser printers, disk controllers, and PBX systems.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram reflects LSI Logic's LR3000.

I—DATA-MANIPULATION INSTRUCTIONS
Implements a traditional load-store architecture. Thus, all data-manipulation operations occur on data in internal registers at the rate of one operation per cycle. Operations are typically in the 3-operand format. These operations include add, subtract, and logical operations, as well as multibit shifts, comparisons, and multiply and divide operations.
II—DATA-MOVEMENT INSTRUCTIONS
Load and store to memory—in RISC CPUs, external memory is only accessed for simple loads and stores. Load and store to CPU registers. Processor supports loading and storing of unaligned 32-bit data.
III—PROGRAM-MANIPULATION INSTR
The processor contains a rich set of instructions for program manipulation and operating-system kernels. These include the coprocessor interface to the MMU to support the virtual memory system. The processor also contains a number of instructions to manage the flow of program control, including numerous branch conditions, SysCall and break instructions, and the ability to interrupt the processor in software. Stack and frame pointer manipulations are performed in software according to the binary conventions of the MIPS compiler suite.
IV—PROGRAM-STATUS-MANIP INSTR
Exceptions can be initiated by interrupt, memory access faults, and the floating-point coprocessor and are tracked by in-system control registers.
V—SYSTEM-LEVEL INSTRUCTIONS
Bits in the Status Register allow the processor to modify the system interface in order to perform special memory system diagnostics.

Specification summary: The R2000/R3000 implements a 5-stage pipeline to achieve a low average clocks per instruction rate. Coupled with a rich instruction set, sophisticated compilers, and high-frequency operation, the R2000/R3000 family achieves very high performance. The IDT 79R3000 features a full cache controller, including on-chip tag comparison and direct control of the cache RAMs. Thus, the 79R3000 achieves 28 VAX MIPS across a range of benchmarks and can perform 60,000 Dhrystones. LSI Logic's LR2000 is available in 12.5- and 16-MHz versions and achieves 8 and 10 VAX MIPS, respectively. Siemens' SAB R2000A delivers 14 MIPS, and the SAB R3000A delivers 22 MIPS.

HARDWARE — SUPPORT — SOFTWARE

MIPS Computer Systems offers several machines for system development. The architecture is supported by a variety of tools, including logic-analysis tools from Tektronix, Arium, and Gould. IDT offers a line of CPU subsystems. IDT also offers a range of development systems—from an add-in board for the Macintosh II through multiple-user Unix-based MIPS systems.

DT provides C, Ada, Pascal, Fortran, Cobol, and PL/1 compilers on the IDT development machine as well as an Ada cross-compiler on the VAX/VMS available from InterACT.
The operating system RISC/os is a merged AT&T System V.3 and Berkeley BSD 4.3 Unix including TCP/IP and NFS networking software. It includes the MIPS optimizing compiler as well as the MIPS symbolic debugger. Pixie, the proprietary MIPS profiling tool, is also part of the Risc/os.
Third-party software provides solutions for a wide variety of applications needs. Refer to the RISCware directory from Synthesis Software Solutions Inc.

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Circle 77 for Literature | **Circle 78 for Sales Contact**

29000 RISC

32-BIT CMOS

AVAILABILITY: Now for 29000 CPU and 29027 arithmetic accelerator.
COST: $150 for the 16-MHz 29000 and $422 for the 16-MHz 29027 (100). Parts are also available in 20- and 25-MHz grades.
SECOND SOURCE: Under negotiation.

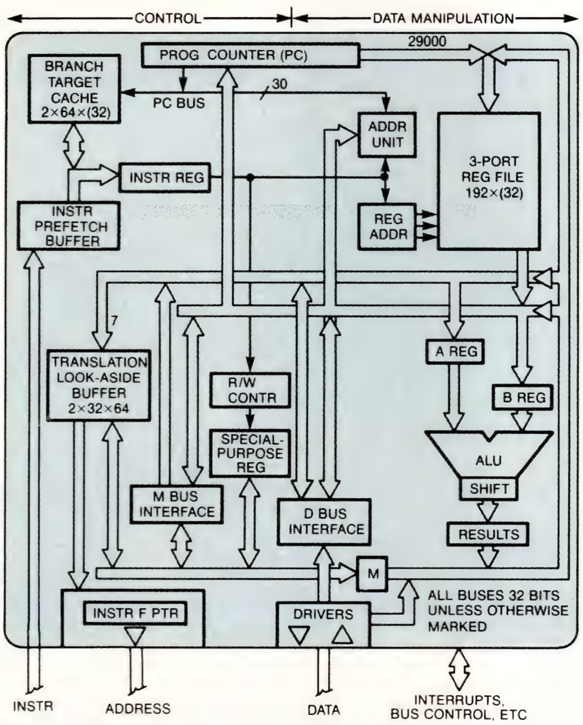
Advanced Micro Devices (AMD)
901 Thompson Pl
Sunnyvale, CA 94086
Phone (408) 732-2400

For more information, Circle No. 403

Description: State-of-the-art implementation of RISC µP concepts with expected stress on obtaining as close to single-cycle operation as possible (even with branching) and a special emphasis on keeping users' system costs down by bus timing, etc, which allows lower-cost external memories. Note that though first two digits of this µP's designation—"29"—are the same as supplier's previous building-block families (see elsewhere in directory), this 29000 family is the architectural opposite. The other building-block families are intended for user-defined (microcoded) complex instruction sets, whereas this µP has a regular, fixed, and purposely simple instruction set; moreover, it is decoded by logic. Companion compilers are an essential part of family.

Status: Over the past 1½ years since its introduction, the 29k has accumulated over 170 design wins. 25 companies have announced their 29k-based products. Areas of particular success for the RISC µP are high-end laser printers; graphics, including graphics controller boards, graphics accelerators, real-time image processing, and medical imaging; and network products, including protocol converters, network node controllers, FDDI networks, and ISDN-related systems.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Burst-mode addressing allows use of lower-cost video RAMs to replace more-expensive, high-speed, static CMOS RAMs, with only moderate loss in performance (14 MIPS sustained vs 17 MIPS).
2. There is a coprocessor interface to companion 29027 floating-point chip. The 29027 uses combinatorial logic, so operations take only five 29000 cycles.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply (step), divide (step).
Extract contiguous 32-bits from the 64-bit funnel shifter.
Logicals, compare, convert floating point (floating point is not currently implemented in hardware but companion floating-point chip 29027 is available).
II—DATA-MOVEMENT INSTRUCTIONS
Register-to-register moves.
Load and store to external memory and I/O.
Load and store multiple registers to/from external memory and I/O.
III—PROGRAM-MANIPULATION INSTR
Jump, call subroutine, and returns.
Branches (with decisions based on Boolean data in general-purpose registers rather than ALU condition codes).
IV—PROGRAM-STATUS-MANIP INSTR
Status register has usual bits to indicate ALU condition.
Exception handling for 64 reserved and 192 user-defined traps.
V—SYSTEM-LEVEL INSTRUCTIONS
Some of the 23 special-purpose registers are for system control, and these are protected and can be set up via software (some also are affected by execution).

Software notes:
1. Total of 115 instructions. All are not yet implemented in hardware, and those that aren't cause traps.
2. Multiply and divide on the 29000 only does one step. The full multiply and divide instruction causes a trap operation at which a compiler can insert a software routine.

Specification summary: 32-bit CPU fashioned after RISC concepts, designed to perform most frequently used, simple instructions in one cycle. Offered with companion compilers intended to take advantage of architectural simplicity and produce code optimized for performance. Also offered with companion floating-point chip, 29027, which in more CISC fashion makes up for crudeness of math instructions (only partial multiplication and division instructions). Features that ensure uninterrupted flow in 29000's 4-stage execution pipeline are single-cycle branching with branch delays and a 512-byte branch-target cache. Main 192-register file has a 3-port configuration so that instruction fields can specify sources for both operands and the destination for the result. 128 of the registers are addressed by a stack pointer that (in conjunction with the compiler) provides a type of "caching" that speeds procedure calling. External memory space is reached by 4G-byte virtual addressing with demand paging. An on-chip 64-entry MMU performs address translation in a single cycle and is flexible so users can choose memory strategy. 25-MHz operating frequency (40-nsec clock period) gives 25-MIPS peak and 17-MIPS sustained performance. Fabricated in 1.2-µm (effective) CMOS with 1.5W power dissipation. Housed in 169-pin PGA.

HARDWARE — SUPPORT — SOFTWARE

The Adapt29K is an in-circuit debugger that allows monitoring and signal tracing on target hardware. The PCEB29K is a personal computer plug-in execution board for software development. In addition, an architectural simulator is provided with the AMD software development package.
From others: Embedded Performance provides the System 29000 emulator. Gould provides the Clas 4000 Logic Analyzer. Hewlett-Packard offers the logic analyzer Am29000 Probe Interface and the AdaptII emulator. Behavioral models are available for CAE workstations from Daisy Systems, Logic Automation, and Teradyne. In addition, VME boards, PC add-in boards, add-in boards for Macintosh computers, and box-level computer systems are available based on the Am29000. A list of third-party support products are summarized in the biannual Fusion29K Catalog published by AMD.

AMD supplies a simulator, debugger, resident debugger, and a cross-development package. AMD has contracted with a "leading" compiler source for optimizing compilers for C, Fortran, Pascal, and Ada. Note that there is an intentional symbiotic relationship between 29000 architecture and compilers. For example, compilers have access to internal 29000 operations, such as pipelining, and thus can insert useful instructions at branch delays. They can also weed out redundancies in loops. Other providers of compilers, translators, and complete tool sets are Embedded Performance, Intermetrics, Irvine Compiler Corp, MetaWare, Microprocessor Services, Microtec Research, Step Engineering, and Verdix Corp. These use the C language and Ada and run on IBM PC/AT-class machines as well as Sun and VAX computers.

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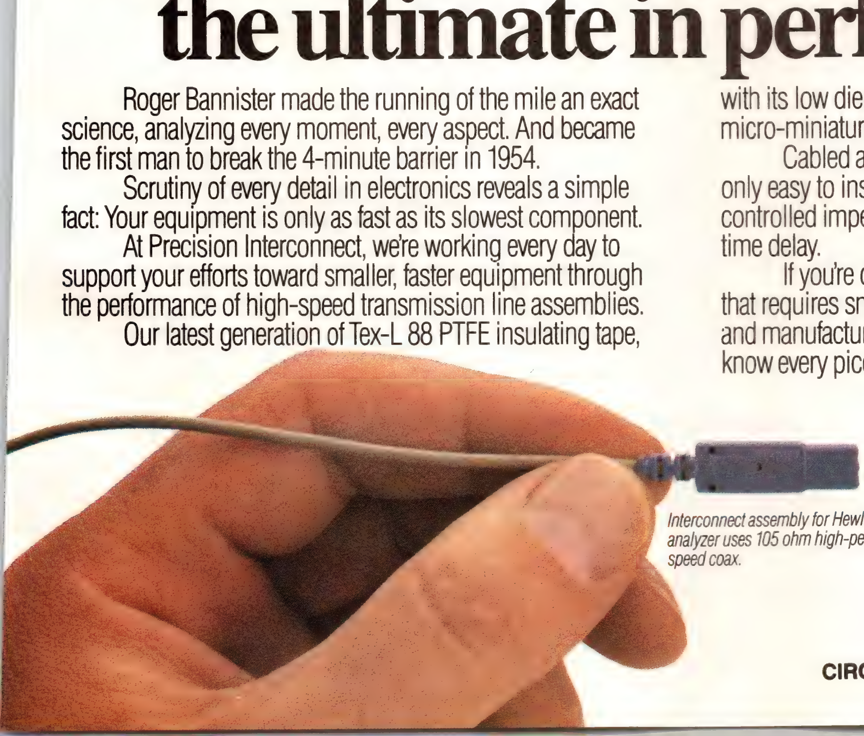

Interconnect assembly for Hewlett-Packard logic analyzer uses 105 ohm high-performance, high speed coax.

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16640 S.W. 72nd Avenue
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CIRCLE NO 59

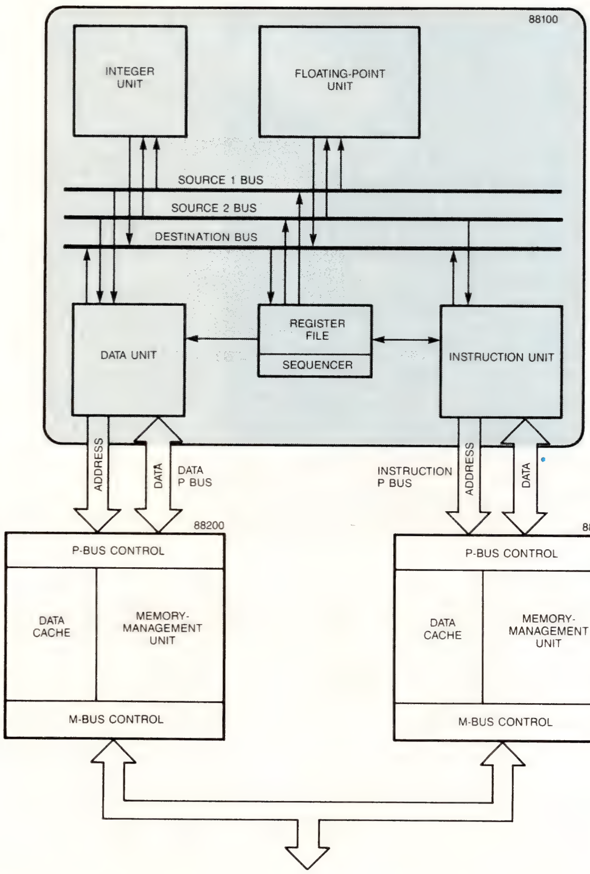
AVAILABILITY: Both the 88100 CPU and the 88200 cache/memory-management unit (CMMU) are available now in 20- and 25-MHz versions. Limited numbers of samples of the 33-MHz μP are available now.
COST: The 88100 costs $495; the 88200 costs $795 (100).
SECOND SOURCE: SGS-Thomson for militarized versions.
CORE: Motorola's architecture can incorporate as many as six special-function units into the 88100 chip.

Motorola Inc
Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (800) 441-2447
For more information, Circle No. 404

Description: The 88000 family is Motorola's entry into the reduced-instruction-set computer (RISC) arena. The 88000 family encompasses the 88100—the CPU—and the 88200—the memory-management unit. The 88100 chip supplies full 32-bit registers, data paths, and addresses. Most instructions take only one cycle or are put in a concurrent execution pipeline in one cycle. The chip also performs standard IEEE-P754 floating-point math operations in one cycle. The corresponding 88200 cache/memory-management unit supports a demand-paged virtual-memory environment. The chip controls two 4G-byte logical address spaces—one for the user and one for the supervisor. The chip's architecture supports multiprocessor operations.

Status: The 88000 μP family was announced in April '88. At the introduction, Motorola not only unveiled its two chips but also produced a list of more than 50 companies that have adopted the 88000 μP family or were developing software for it. Further bolstering the position of the nascent 88000, an independent group of manufacturers has already founded the 88open Consortium Ltd (Stratham, NH) to support and promote the μP family. More than simply a promotional trade group, the consortium develops standards, like the Binary Compatibility Specification, which allows applications written for the 88000 to execute on all 88000 hardware.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Architecture shown is for the 88100. The CMMUs are shown in block-diagram form.
2. The P bus supplies the interface between the 88100 and either local memory or an 88200 CMMU. The synchronous P bus operates at the same clock rate as the 88100. Peak data rate is 80M bytes/sec.
3. The 88100 includes 32 general-purpose registers.

I—DATA-MANIPULATION INSTRUCTIONS
The integer-math instructions include add, subtract, divide, multiply, and compare. There are equivalent floating-point instructions as well as integer-float conversion, store, exchange, round, and truncate instructions. The instructions also provide logical and bit-field operations.
II—DATA-MOVEMENT INSTRUCTIONS
The basic data-movement instructions let the CPU load registers, addresses, and the control register's contents. The CPU can also store information and exchange the contents of registers and memory. The instruction set includes operations that move data within the floating-point math unit.
III—PROGRAM-MANIPULATION INSTR
These instructions include conditional and unconditional branch, jump, and subroutine-call commands. The 88100 also provides trap instructions that check bit locations, memory boundaries, and interrupt conditions.
IV—PROGRAM-STATUS-MANIP INSTR
The 88100 can process exceptions—those conditions that cause the processor to stop its operation and locate a potential problem. Exceptions include interrupts, memory-access faults, math errors such as divide by zero, and trap instructions.

Specification summary: The 88100 provides register-to-register operations for all data-manipulation instructions. Separate source and destination registers are available. The CPU supports register-to-register and register-plus-immediate-value address modes. Because address calculations are quick, memory-access operations are speedy, in keeping with the RISC philosophy. The CPU employs delayed branching, which reduces pipeline delays due to a change in program flow. The 88200 incorporates 16k bytes of cache memory as well as cache-control logic, memory-management logic, and bus-control circuits. Multiple CMMUs can operate in parallel. Both the 88100 and 88200 come packaged in 180-pin PGA packages. The chips operate over the standard 0 to 70°C temperature range.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: The company has announced its Platform-88 ($39,500) for system developers. The computer should be available for shipment now.
From others: Various 88000 hardware is available from Beacon Technologies (Valparaiso, FL); Golden Triangle Computers Inc (San Diego, CA); Integrated Micro Products Ltd (Durham, UK); Tadpole Technology (Cambridge, UK, and Dublin, CA); and Tektronix Inc (Beaverton, OR).

From Motorola: The Platform-88 computer runs Motorola's Unix System V.3 as well as other languages and development tools such as an assembler, a code scheduler, and optimizing C and Fortran compliers.
From others: A variety of compilers and applications are available for the 88000. See the 88open software catalog.

80960 — 32-BIT CMOS

AVAILABILITY: 16-, 20-, and 25-MHz 80960KA and KB in PGAs in production; 16-MHz plastic quad flatpack (PQFP) sampling. 16-, 20, and 25-MHz '960MC in PGAs and QFPs in production. The '960CA is sampling now, production is scheduled for fourth qtr '89.
COST: Prices depend upon speed, package, and temperature range, but in 1000s, range from $94 to $158 for the '960KA, $179 to $285 for the '960KB, $920 to $1220 for the '960MC, and $213 to $325 for the '960CA.
SECOND SOURCE: Internally sourced from three different Intel facilities.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

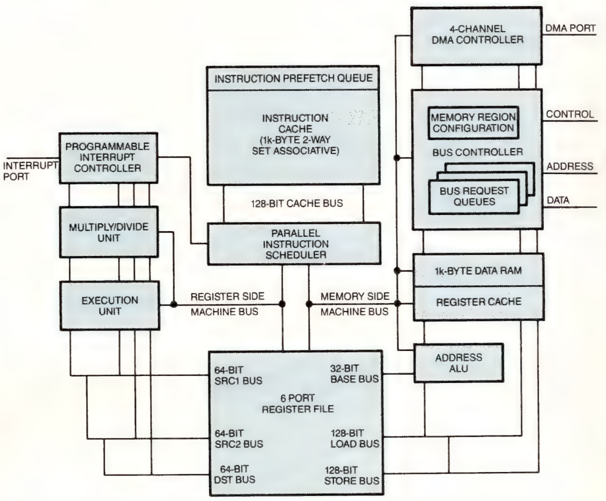
For more information,
Circle No. 405

Description: The 80960 is Intel's 32-bit family of µP chips that has been designed specifically for embedded-control applications. There are four upwardly compatible versions of the RISC-based architecture. The family includes the basic 80960KA core version, which provides 6 to 12 VAX MIPS (depending on frequency); the 80960KB, which includes an on-chip floating-point math unit; the 80960MC, which comes with on-chip memory-management/protection and multiprocessor support; and the 80960CA, which features a software-configurable pipelined bus, 1.5k bytes of on-chip data RAM, a 1k-byte, 2-way set-associative instruction cache—which you can lock for real-time operation—and a 4-channel chaining DMA processor. The '960MC is a military version of the chip, which supplies multiprocessing and Ada-tasking support.

Status: Since the 80960 family's introduction, the family has enjoyed widespread acceptance in a broad spectrum of commercial and military designs. The 80960 family played a role in legitimizing 32-bit embedded control as an important market. Intel's approach is family oriented; not only is there a wide range of 32-bit CPU solutions at different price/performance levels, but also 80960-specific support components such as the 27960 burst EPROM and 85C960 bus control component. Intel claims the total "kit" approach exists to serve embedded-control customers with an easy-to-design-with set of CPU and peripheral parts. The 80960 architecture scored a key endorsement when it was chosen as one of two 32-bit instruction set standards by the military to succeed the 16-bit 1750A standard.

CHARACTERISTICS

HARDWARE



Hardware notes:
1. Unlike other RISC processors, the '960 provides only one data bus for instructions and data. The bus multiplexes address and data information.
2. The basic '960 chip includes 16 32-bit global registers and 16 32-bit local registers. The stack requires one global and three local registers for housekeeping operations.
3. The floating-point math unit (80960KB) operates from four 80-bit registers.

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Bit operations, unsigned and signed byte, unsigned and signed half-word (16-bit quantity), unsigned and signed word operation. All CPUs have hardware multiply/divide unit. Extended arithmetic support allows math operations on operands larger than one word. Floating-point operations on single-, double-, and extended-precision operations are supported in hardware on the KB and MC versions.
II—DATA-MOVEMENT INSTRUCTIONS
Bytes, half words, words, double words, triple words, and quad words can be moved to and from memory. Memory operations are supported by a full complement of addressing modes, including IP relative. All CPUs support unaligned memory operations.
III—PROGRAM-MANIPULATION INSTR
Both Berkeley and Stanford forms of subroutine call, return; several types of branch instructions. Full set of conditional tests, including bit test and jump.
IV—PROGRAM-STATUS-MANIP INSTR
Process control word and arithmetic controls can be modified under program control.
V—SYSTEM-LEVEL INSTRUCTIONS
Seven different types of trace controls. Hardware and software breakpoints. 80960CA has operations to program DMA channels and control hardware features such as locking the cache. 80960MC has operations to directly support shared memory multiprocessing.

Specification summary: The 80960KA has a 512-byte instruction cache, a 256-byte register cache, and a 4-input interrupt controller. The 80960KB is socket compatible with the 80960KA but features an on-chip IEEE-P754-compatible floating-point unit. The 80960MC adds an MMU and multiprocessing support to the features of the KB. Finally, the 80960CA allows multiple-instruction-per-clock execution and offers a 4 clock-cycle 32-bit multiplier, 8 interrupt inputs, a 1k-byte lockable instruction cache, 1.5k bytes of on-chip RAM, a register cache configurable to 15 levels, 4 DMA channels, and a software-configurable bus.

SUPPORT

HARDWARE

From Intel: The EVQT960E ($960) with 256k bytes of 2-wait-state memory and the EVQT960F ($1960) with 256k bytes of zero-wait-state memory are serially hosted evaluation and prototyping boards for the 80960KA/KB. The EVA960KB board ($4500) is a PC/AT-compatible board with onboard debug monitor and up to 4M bytes of dynamic RAM. The EXV960MC board ($9000) is a 25-MHz Multibus I development board for military and Ada applications. The EV960CA is an evaluation board for the 80960CA. ICE960KB ($16,495) is available for the 80960KA/KB.
The 85C960 is a bus control chip for the KA/KB; the 27960CX/KX are high-speed burst EPROMs for the 80960KA/KB/CA; the 27C202 is a high-speed 16-bit-wide EPROM for the KA/KB/CA. The 82380 is a multifunction peripheral with timer-counters, 8 channels of DMA, and 15 interrupt inputs that can interface to the '960KA/KB/MC. The M82965 is a bus interface component that provides multiprocessing and fault tolerance support for the 80960MC. Intel provides a number of public-domain designs using all of these components.
From others: 80960CA Multibus II boards are available from Micro Industries. 80960CA VME boards are available from Heurikon ($3995) and Tadpole. Fluke provides logic-analyzer support.

SOFTWARE

From Intel: ASM960 ($900 for the PC/AT) includes an assembler and linker for the '960 family. iC960 ($700 for the PC/AT) is a full ANSI C compiler for the '960 family. Gen960 builds memory images for the KA/KB/MC/CA. Hosts include the PC/AT, Sun3, VAX/VMS. Ada960 ($28,000 and up) is available for VAX/VMS. RMK960 ($1500) is a real-time kernel for 80960KA/KB. SIM960CA ($750, PC/AT) is a software simulator for the 80960CA. DB960 ($2500) is a C source-level debugger hosted on a PC/AT for both the KA/KB and CA targets.
From others: Wind River VxWorks provides a full-featured operating environment that includes file system support, TCP/IP networking. Ready Systems VRTX32 ($4810) provides a deterministic real-time kernel for the 80960 family. Microtec Research provides a complete 80960 tool chain, from C compiler through XRay debugger. QTC provides an instruction scheduler/optimizer for the 80960CA. The Solutions960 catalog from Intel describes additional 80960 tools and applications.

AVAILABILITY: The 33-MHz version will be available in the fourth qtr '89. Samples are currently available.
COST: The 33-MHz i860 costs $750 (1000).
SECOND SOURCE: None.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

For more information,
Circle No. 406

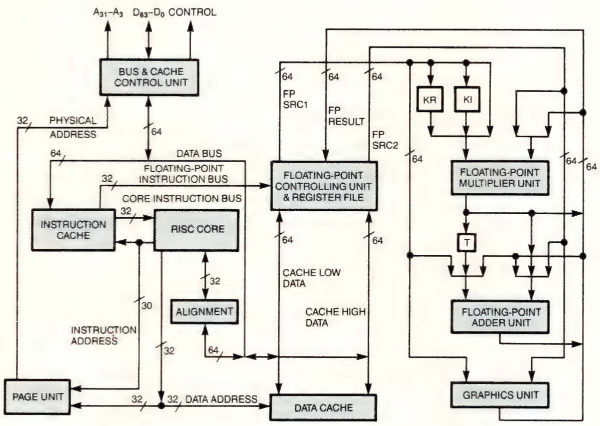
Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

For more information,
Circle No. 407

Description: The i860 CPU is a 64-bit µP designed to provide balanced performance across integer, floating-point, and 3-D graphics operations. The µP incorporates a RISC integer unit, a floating-point adder, a floating-point multiplier, an 8k-byte data cache, a 4k-byte instruction cache, a paging and MMU, and a 3-D graphics unit. The i860 runs Unix but is not designed to run 386 software.

Status: 33- and 40-MHz samples are available now. Volume production is scheduled to begin late this year. The i860 has amassed more than 50 design wins to date in supercomputer, minicomputer, 3-D graphics workstation, and application accelerator designs. Multiprocessor version of Unix/System V rel 4.0 will be available in 1990.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Integer arithmetic, logicals, and shifts. Integer multiply. IEEE-754 floating-point add, subtract, multiply. Single and double precision, and conversions between. Reciprocal and square-root seed instructions. Special "dual operation" floating point allows 2 operations per clock. Graphics instructions for pixel interpolation and Z-buffer check.
II—DATA-MOVEMENT INSTRUCTIONS
16-, 8-, and 4-byte floating-point loads and stores, with variable strides and autoincrement. 4-, 2-, and 1-byte integer loads and stores. Transfers between integer and floating-point registers. Special load instruction assists data caches. Pixel-store operation of 8 bytes.
III—PROGRAM-MANIPULATION INSTR
Unconditional and conditional branches, both "delayed" and nondelayed forms. Single-cycle loop control operation. Indirect call and indirect branch. Dual instruction mode allows execution of 2 instructions per clock.
IV—PROGRAM-STATUS-MANIP INSTR
Data breakpoint register for breakpoint debugging. Big-endian mode bit switches between access modes. Cache-control bits for cache locking and testing.
V—SYSTEM-LEVEL INSTRUCTIONS
Lock/unlock instructions for semaphores. Flush instruction for write-back data cache. Single-cycle translation look-aside buffer and instruction cache invalidate.

Specification summary: Information not provided by manufacturer.

HARDWARE — SUPPORT — SOFTWARE

From Intel: Information not provided by manufacturer.

From Intel: Information not provided by manufacturer.

2900, 29C00, 29G00 BIT SLICE

4-BIT × N, 16-BIT, 32-BIT; BIPOLAR, CMOS, AND GaAs

AVAILABILITY: Now for bipolar parts and most CMOS variations on 2900 theme. Varies for latest highest speed and widest data-word versions.
COST: $6 for 2901A/B/C (100); $20 for 2903A (100). See table for others. Prices for CMOS similar.
SECOND SOURCE: None for original bipolar 2900. For new CMOS versions: IDT, Cypress, Wafer Scale Integration, Logic Devices, and others. Vitesse (29G01) has a $61 (100) 80-MHz GaAs version.
CORE: Most of the sources for CMOS 2900 also have either the family parts in their cell library or intend to have them. In addition, there are companies, such as VLSI Technology, that may not have standard 2900 parts, but still have them in their cell libraries.

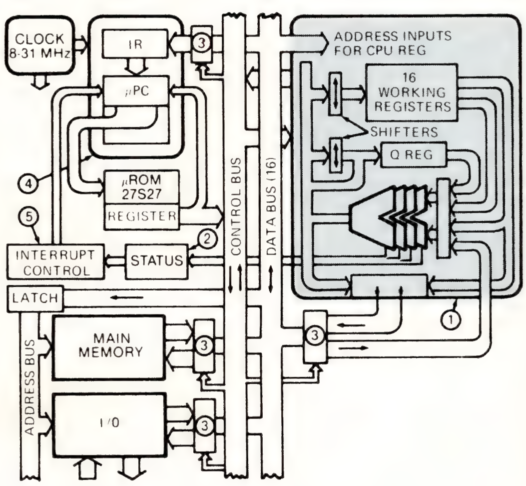
Description: Ever-growing and changing family of mostly TTL bus-compatible, bit-slice building blocks. By now almost all possible semiconductor technologies are being used: bipolar (both TTL and ECL internally), CMOS, and even GaAs. Intended for microprogrammable systems in which they emulate existing computers or for use in specialized digital controllers. Latest twist is to use them as macrocells in semicustom libraries.

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94086
Phone (408) 732-2400

For more information, Circle No. 399

Status: This bit-slice family has been around a long time. Each time its life seems over, it is reborn. Now it's getting new life from CMOS versions from many different sources. These versions have almost the same speed as the original bipolar—some suppliers claim equal or better speed—and only a fraction of the power consumption. The architectural motivation usually is to attain higher levels of parallelism with wide microinstructions, in which many fields control different hardware blocks. In many instances the CMOS versions are part of macrocell libraries, so that they can be assembled (ideally by a customer engineer at his or her workstation) into single-chip or few-chip semicustom VLSI solutions. The 2900 family is never likely to see especially high unit volumes because parts costs are too high.

HARDWARE — CHARACTERISTICS — SOFTWARE



Specification summary: TTL bus-compatible building blocks for creating moderately high-performance computers and controllers. Slices were originally 4 bits wide but now can be as much as 32 bits wide. Parts include sufficient features for emulating most computer architectures. User defines end product's macroinstruction set by microprogramming ROM. RALUs (2901, 2903, and 29203) respond to 8 and 16 basic instructions (2903 and 29203 include multiply and divide and floating-point normalization) within one clock cycle of 50 to 125 nsec (2901C performs 16-bit add in 83 nsec). Original family parts fabricated entirely from Schottky TTL. Now fine-geometry (near 1 μm) CMOS can produce equivalent speeds at lower power consumption. With CMOS, there's a trend to consolidate multiple 2900 functions on chip and to go to new space-saving packages.

User defines macroinstruction set by microprogramming ROM. Parts respond to the following instructions:

I—DATA-MANIPULATION INSTRUCTIONS
2901 performs three arithmetic functions on two operands, as well as five logic functions.
2903A performs seven arithmetic functions and nine logic operations, as well as multiply and divide. Simultaneous add (or subtract) and shift possible.
29203 has floating-point-normalize instruction.

II—DATA-MOVEMENT INSTRUCTIONS
16 working registers in RALU RAM can be addressed two at a time for supplying two operands to the ALU simultaneously.

III—PROGRAM-MANIPULATION INSTR
Defined by user in microcode. 2930 program-control unit executes 32 fetch and branch instructions.

IV—PROGRAM-STATUS-MANIP INSTR
2904 shift and status-control chip provides two status registers for the 4-bit carry, overflow, zero, and negative. Bits can be set or cleared. Shift through carry or overflow. Borrows can be stored for subtract.

BASIC 2900 PARTS

PART	# ON DIAGRAM	DESCRIPTION	COST (100 QTY)
2901/B/C	1	ALU	$6
29C01			$6
29C101			$35
2902A			$1.80
2903/A			$20
29203		ALU (BCD)	$20
2904	2		$16
29705/A		2-PORT RAM	$10
2909/A	4	MICROPROGRAM CONTROL UNITS	$5
2910/A			$13
29C10A			$13
2911/A			$4
29803A			$4
29811A			$3
2930		PROGRAM CONTROL UNITS (RELATIVE ADDRESSING)	$20
2932			$18
2913		INTERRUPT	$5
2914	5		$10
2905	3	TRANSCEIVERS	$5
2906			$7
2907			$4
2915A			$5
2916A			$4
2917A			$4

HARDWARE — SUPPORT — SOFTWARE

From third parties: Step Engineering (Sunnyvale, CA) offers new lower-cost PC XT/AT-based Microstep microcode development station ($3695). It consists of plug-in card for PCs containing 25-nsec RAMs to simulate a 128 × 4k-bit microcode ROM plus debug/control software. It would be used in conjunction with Step's Metastep Microprogram language ($3000, or $6195 bundled with Microstep). Step's full-fledged Step-40 is expensive, but it has 10-nsec, 512 × 64k-bit microcode ROM. Hardware tools also available from HiLevel Technology (Tustin, CA) and others.
For ASIC: Silicon compilers for members of 2900 family (2901, 2910, 2913, and 2940) are in VLSI Technology's compiler library.

From third parties: Step Engineering (Sunnyvale, CA) offers Metastep, a generalized software language for developing microcode ($3000). It runs on CPM/68K, MS/DOS, VAX/Unix, and VAX/VMS. It is claimed to have the flexibility and structure to greatly ease the tedious and error-prone software side of microcode system development. Software tools also available from HiLevel Technology (Tustin, CA) and others.
Literature: *Bit Slice Microprocessor Design,* by John Mick and Jim Brick, McGraw-Hill, NY, NY, 1980.

29300, 29C300 — 32-BIT BIPOLAR AND CMOS

AVAILABILITY: 29300 and C300 available now in several speed grades. 29400 ECL discontinued in favor of advanced CMOS.
COST: A set of 29300 chips costs less than $350.
SECOND SOURCE: None directly but, especially for CMOS parts, TI and Weitek offer 32-bit building blocks.

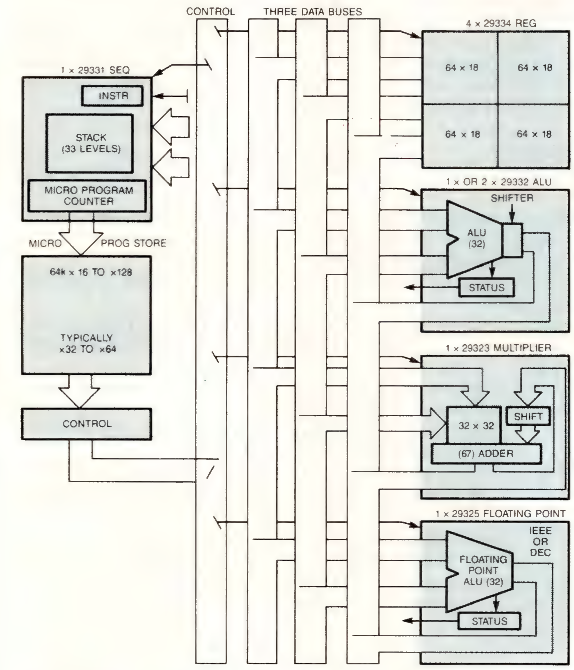
Description: 32-bit bipolar and CMOS building-block chip set that follows concepts established by 2900 bit-slice family, but with two major differences. First, family members all have a fixed, 32-bit data width. Second, the architecture and resulting microinstruction set are optimized for easy compiler writing. State-of-the-art performance has been achieved, as indicated by 70-nsec microinstruction cycle times and a 32 × 32-bit multiplier (50 nsec).

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94086
Phone (408) 732-2400

For more information, Circle No. 400

Status: Supplier is sitting on both sides of the RISC-CISC, high-performance 32-bit debate: the 29000 RISC μPs and the 29300 μPs. RISC chips use combinatorial logic to get instructions down to single-cycle execution. The 29C300 also executes instructions in a single cycle, but implementing complex instruction sets on the C300 requires a 70-nsec clock cycle. The 29000 RISC family can operate faster.

HARDWARE — CHARACTERISTICS — SOFTWARE



PART NUMBER	DESCRIPTION	PERFORMANCE	AVAIL-ABILITY	COST (100 QTY)
TTL				
29331	16-BIT SEQUENCER	75 nSEC	NOW	$88
29332	16-BIT ALU	75 nSEC	NOW	$220
29334	84×18 REG FILE	24 nSEC	NOW	$80
29337	BOUNDS CHECKER	20 nSEC	NOW	$22
CMOS				
29C323	32-BIT MULTIPLIER	100 nSEC	NOW	$119
29C323-2	32-BIT MULTIPLIER	50 nSEC	NOW	$238
29C331	16-BIT SEQUENCER	90 nSEC	NOW	$72
29C331-2	16-BIT SEQUENCER	70 nSEC	NOW	$99
29C332	32-BIT ALU	80 nSEC	NOW	$175
29C334	64×18 REG FILE	30 nSEC	NOW	$54
29C334-2	64×18 REG FILE	20 nSEC	NOW	$86
29325/12	32-BIT SINGLE PRECISION	120 nSEC	NOW	$99
29325A	32-BIT SINGLE PRECISION	70 nSEC	NOW	$269
29C325/12	32-BIT SINGLE PRECISION	120 nSEC	1988	$99
29C327	64-BIT DOUBLE PRECISION	125 nSEC	1988	$329

NOTE:
'325 AND '327 PERFORMANCE SPEC REFERS TO CLOCKED MULTIPLY TIME.

Hardware notes:
1. Many different architectures possible because of flexibility of parts.
2. Possibility of sharing dual-ported registers between two ALUs so that address calculation and data manipulation occur simultaneously within cycle. (Each ALU would have its operands and result read and written into a common multiported register file.)
3. Deep pipelining avoided so there can be fast response to decisions.

I—DATA-MANIPULATION INSTRUCTIONS
For 29332 ALU: includes 64-bit n-bit shift-up/down funnel shifter that can be combined with logic functions. Multiply and divide (one bit at a time). Priority encoding to support floating-point operations and graphics.
For 29325 floating point: efficient execution of Newton-Raphson division and Horner's method of polynomial evaluation. Both IEEE and DEC formats (addition, subtraction, multiplication) with conversion between two modes.
For 29323 32 × 32-bit multiplier: single- or double-precision multiply in one or four cycles, respectively.
II—DATA-MOVEMENT INSTRUCTIONS
For 29334 64 × 18-bit register file (cascaded for full word width and desired length and used in conjunction with ALU): individual write for byte, 16-bit half word, or 32-bit full word.
III—PROGRAM-MANIPULATION INSTR
For 29331 microprogram sequencer: instructions designed to support high-level-language constructs.
The 33-level stack supports interrupts, loops, subroutine nesting, and multitasking at microlevel.
Microtrapping for reuse of prior microinstruction.
No support for relative addressing, because designers wanted to avoid performance penalty of adder, but decisions and interrupts handled on chip for fastest response.
IV—PROGRAM-STATUS-MANIP INSTR
Status registers in ALU, floating point, etc.

Software notes:
1. Designers say they endeavored to keep instructions orthogonal and symmetrical to ease task of compiler writing and facilitate structured microprogramming.
2. Self-checking implemented by parity bits in register file and by parity in off-chip data paths and ability to parallel units and compare results.

Specification summary: Building blocks for 32-bit-wide microprogrammable computer systems. Core set includes five parts (see table) that can stand alone or be used in mixed systems. Architecture supports features needed on advanced minicomputers, like parity checking and master/slave functional comparisons. Also suited for direct, very fast execution of high-level languages via compiled microcode. Triple data-bus architecture, with unidirectional buses for minimum speed loss caused by bus turnaround. Architecture sufficiently open to allow inclusion of performance accelerators. Family includes floating-point unit and 1-cycle fixed-point multiplier. TTL packages incorporate three low-profile horizontal fins to handle 4 to 7W heat dissipation. CMOS versions will dissipate in the 1W range and will not require heat sinks or cooling airflow.

HARDWARE — SUPPORT — SOFTWARE

From third parties: Step Engineering offers new lower-cost PC XT/AT-based Microstep microcode development station ($3695). It consists of plug-in card for PCs containing 25-nsec RAMs to simulate a 128 × 4k-bit microcode ROM plus debug/control software. It would be used in conjunction with Step's Metastep Microprogram language ($3000, or $6195 bundled with Microstep). Hardware tools also available from HiLevel Technology and others.

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Text continued on pg 190

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Model MSK 10-10M

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The preview switch (d-c on-off) allows you to pre-set voltage and current with the digital meters displaying the set values. At "d-c off", no voltage is applied to the output terminals and no load current needs to be drawn to set the current control. At "d-c on", the set voltage is applied to the output terminals. The appropriate mode indicator is lit, and the meters indicate *actual* voltage and current.

Series MSK power supplies use fully dissipative, high gain linear (series pass) stabilizer circuits, for low noise output, good stability, and accurate resettability. A built-in quiet, low-speed fan ensures good cooling in the crowded environment of your laboratory.

100 WATT MODELS

MODEL	d-c OUTPUT RANGE		POWER
	Volts	Amps	Watts
MSK 10-10M	0-10	0-10	0-100
MSK 20-5M	0-20	0-5	0-100
MSK 40-2.5M	0-40	0-2.5	0-100
MSK 60-2M	0-60	0-2	0-120
MSK 125-1M	0-125	0-1	0-125

DIMENSIONS: 5¾"*H x 8⅛"W x 13⁵⁄₃₂"D *including feet
NET WEIGHT: MSK 10-10M, 20-5M, 40-2.5M, 60-2M . . . 19 lbs. MSK 125-1M . . . 22 lbs.

STATIC SPECIFICATIONS

INFLUENCE QUANTITY		VOLTAGE MODE	CURRENT MODE
SOURCE 105-125/210-250V a-c		0.01%	0.01%
LOAD No load – full load		0.01%	0.05%
TIME 8-hour (drift)		0.01%	0.02%
TEMPERATURE Per °C		0.01%	0.02%
RIPPLE and NOISE	rms	0.5mV	0.02%
	p-p	3.0mV	0.01%

Note: Percentage values are referenced to the maximum rated voltage or current of the unit.

For complete specifications send for MSK brochure 146-1619.

MPS 620M™ TRIPLE OUTPUT

This power supply has been specifically designed to meet the needs of the IC/microprocessor experimenter.

The MPS 620M is actually two linear (series pass) power supplies in one: The first has a single 0-6V, 0-5A output for digital work; the second has two *tracked* outputs, 0 to +20V and 0 to −20V, both rated at 0-1Amp. The two power supplies are completely isolated from each other, sharing only the front panel meters and the chassis.

The 0-6V output is continuously adjustable with a 10-turn control on the front panel, and is backed up by a current limiter and overvoltage crowbar. The crowbar is set by a locking-type screwdriver adjustment. The fixed rectangular current limit circuit is set to approximately 110% of maximum current. The dual 0 to ±20V outputs are continuously adjustable by a single 10-turn front panel control, and tracking is better than ±1% +10mV. The outputs can be used in series to provide 0-40V, but since they share a common (center) terminal, they cannot be used in parallel. Both outputs are equipped with adjustable current limits.

70 WATT MODEL

OUTPUT	VOLTS	AMPS
Output #1	0 to 6	0-5
Output #2	0 to +20	0-1
Output #3	0 to −20	0-1

Outputs 2 and 3 are tracked.
Output 1 is protected by an overvoltage crowbar.

DIMENSIONS: 5⁷⁄₃₂"H x 12¹⁷⁄₃₂"W x 12⅞"D **NET WEIGHT:** 29 lbs.

STATIC SPECIFICATIONS

INFLUENCE QUANTITY		OUTPUT EFFECTS 0 to 6V Output	OUTPUT EFFECTS 0 to ±20V Output
SOURCE 105-125/210-250V a-c		0.01%	0.01%
LOAD No load – full load		0.01%	0.05%
TIME 8 hour (drift)		0.01%	0.01%
TEMPERATURE Per °C		0.01%	0.01%
RIPPLE and NOISE	rms	0.1 mV	0.1 mV
	p-p	1.0 mV	1.0 mV

For complete specifications send for MPS brochure 228-0802.

Data subject to change without notice.

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MSK 20-5M	0- 20V	0- 5A
MSK 40-2.5M	0- 40V	0- 2.5A
MSK 60-2M	0- 60V	0- 2A
MSK 125-1M	0-125V	0- 1A

Along with the usual remote error sensing, Kepco's MSK have a unique preview feature by which you can set the voltage and current before applying power to your load. Meters are LCD, the controls are high resolution 10-turn types. The warranty is 5-year.
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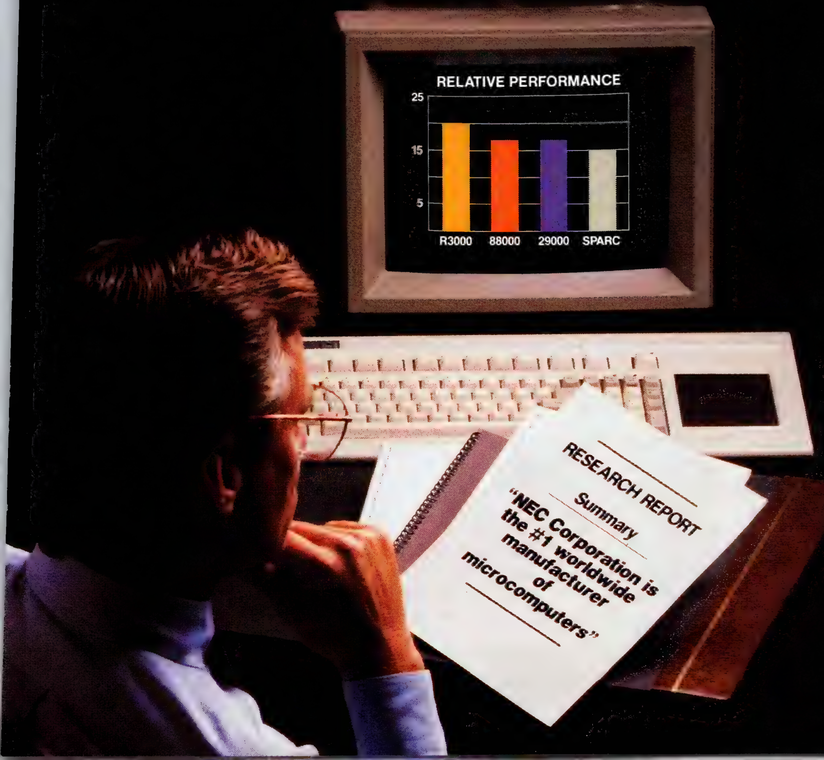
5 *SAMPLES NOW*

Four good reasons deserve another: Samples of the VR3000 and VR3010 are available now along with technical documentation and applications engineering support so you can start building real-world systems that meet the demands of your customers.



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1-800-632-3531/1-415-965-6158

CIRCLE NO 79

NEC

74ACT8800 | 32-BIT CMOS

AVAILABILITY: See table.
COST: See table for prices.
SECOND SOURCE: None.

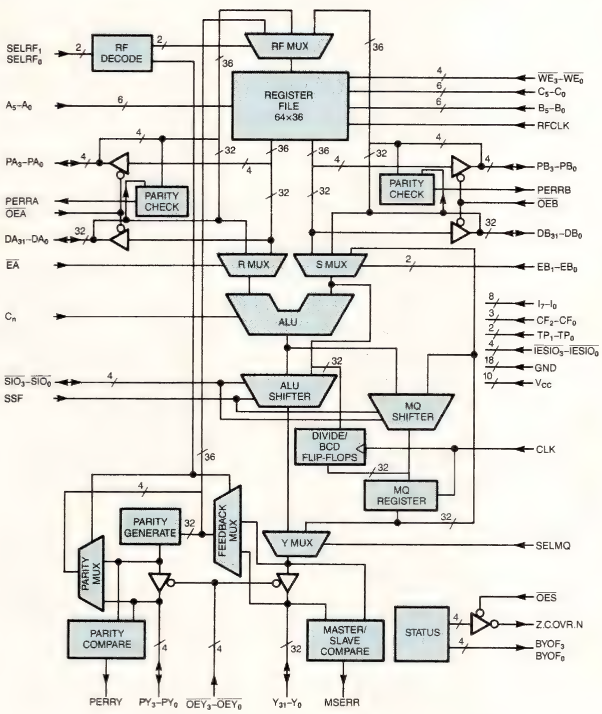
Texas Instruments Inc
Box 809066
Dallas, TX 75380
Phone (800) 232-3200, ext 700

For more information, Circle No. 401

Description: 32-bit processor building-block circuits composed of single-chip VLSI processor functions, all of which are designed for complex processing applications. Instruction cycle times of 50 nsec or less are achieved; low power consumption is attained with the vendor's Epic CMOS technology.

Status: The Act8800 family of building block products competes with similar offerings from Weitek, AMD, and BIT. Future competition could include ASICs. The vendor claims that RISC chips don't currently offer the architectural flexibility to achieve the high levels of parallelism necessary for the RISC chips to compete with the Act8800.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram represents the 8832 32-bit registered ALU. Family architecture facilitates the high degree of system parallelism possible with "wide" microcoding, allowing designer to operate devices simultaneously for greater throughput.
2. All devices are low-power CMOS.

Specification summary: Building blocks for microcoded custom CPU architectures. All devices use TI's Epic CMOS process. The architecture is designed to support high-performance minicomputer, workstation, and graphics machines by incorporating features like parity generation/checking and master/slave operation for tandem processing. Worst-case cycle times of 50 to 75 nsec can be accomplished with relatively low power dissipation. Large-pin-count devices (see table) are packaged in pin-grid arrays and plastic leaded chip carriers.

I—DATA-MANIPULATION INSTRUCTIONS
For 8832 RALU:
50-nsec cycle times, with simultaneous ALU and register manipulate operations.
For 8836 MAC:
Performs 32×32-bit multiply/accumulate in flow-through mode in 48 sec (max) or can be pipelined for 30 nsec (max) operation. Signed, unsigned, or mixed-mode operations.
For 8847 FPU:
Meets IEEE standard for single- and double-precision formats. Performs floating point and integer add, subtract, multiply, divide, square root, and compare.
II—DATA-MOVEMENT INSTRUCTIONS
For 8832 RALU:
3-operand 64W×36-bit register file on chip supports byte-oriented operands for variable data-word widths. 36-bit width = 32 bits data + 4 parity bits. On-chip parity generation/checking.
For 8841 Digital Crossbar Switch:
64 bidirectional data I/Os in 16 4-bit groups. Two selectable hardwired switching configurations. Selectable stored data or real-time inputs.
III—PROGRAM-MANIPULATION INSTR
For 8818 Microsequencer:
Facilitates high-level-language constructs; deep 65×16 stack supports interrupts. Performs multiway branching, conditional subroutine calls, and nested loops.
IV—PROGRAM-STATUS MANIP INSTR
For 8818 Microsequencer:
Decrement loop counter and branch instructions. $\overline{CC}$ input allows conditional branching based on external status.

Software note: Instructions described are for 88XX family devices. 8XX instructions are a subset, and the two sets are completely compatible.

HARDWARE — SUPPORT — SOFTWARE

TI offers the 8800 Software Development Board Design Kit as an evaluation and training tool. The kit includes a board assembly, user's guide, floppy disk with tools written in Microsoft C, and microcode definition files for use with microcode development tools. Built on a PC/AT card occupying a single slot, the 8800 SDB contains an Act8818 microsequencer, an Act8832 RALU, and an Act8847 floating-point unit/integer unit, along with 32k×128 bits of microcode memory. The board operates under an MS-DOS environment.

TI offers functional evaluation modules for the Act8800 family, which are written in Microsoft C and can be used in stand-alone mode or as callable functions. These models correctly represent device timing in clock cycles, measured from the input of control and data to the output of results and status.
Behavioral simulation models for the Act8800 family are available. These models have the timing control and error-handling capability to perform pc-board and system simulation. They also contain an expert debugger. Behavioral models are available from Logic Automation Inc (Beaverton, OR) and Quadtree Software (San Jose, CA).

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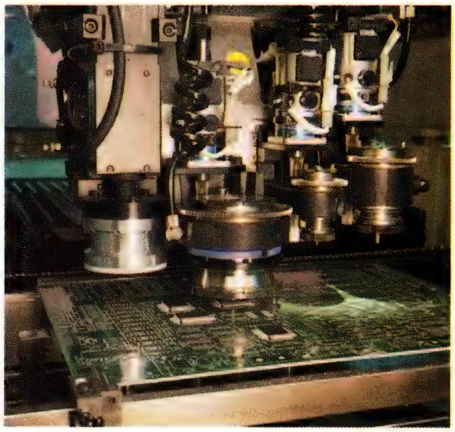

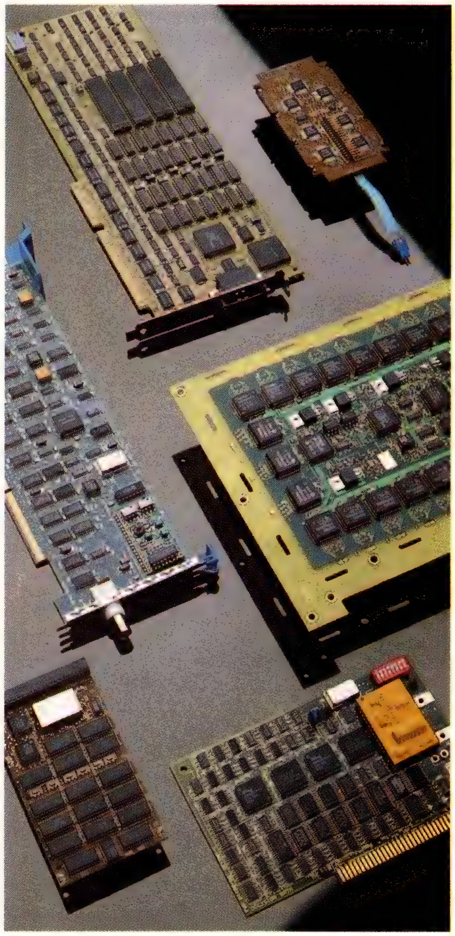

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CIRCLE NO 80

WORD-SLICE GP NUMERIC PROCESSOR

16-BIT CMOS μP BUILDING BLOCKS

AVAILABILITY: Now for most parts; see table.
COST: $20 to $300; see table.
SECOND SOURCE: No direct source, except for industry-standard multipliers. Similar functions are available from AMD, Cypress Semiconductor (San Jose, CA), Integrated Device Technology (Santa Clara, CA), Wafer Scale Integration (Fremont, CA), Weitek (Sunnyvale, CA), and many others.

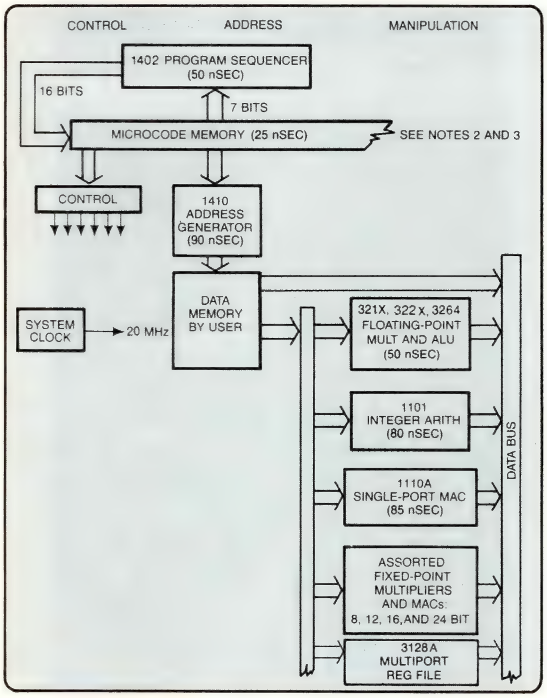
Description: Follows trend established with 2900 bit-slice family of providing building blocks that system designers can use in microprogrammed systems. This family has been found suitable for general numeric or number-crunching applications, such as accelerators. Supplier's goal was to provide microprogram sequencers and address generators that could be used with supplier's floating- and fixed-point multipliers to design complete systems.

Analog Devices Inc
Digital Signal Processing Div
Box 9106
Norwood, MA 02062
Phone (617) 329-4700

For more information, Circle No. 402

Status: These parts are available now.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Architecture shown is only one of many possibilities.
2. Microcode memory can be 64k deep. It can be as wide as designer needs for simultaneous control of one or more data pipes (typically approximately 100 bits).
3. Microcode memory can be RAM for downloading of algorithms from host.

Specification summary: Microprogrammable chips set for numerical processing, permitting increased throughput by user-developed parallelism. Consists of various multipliers and multiplier accumulators (see table) and microcode program sequencers and address generators (see table). It can be driven by a 10-MHz clock, and within resulting 100-nsec cycle, can perform complete instructions (obtain data from memory and process it). Most recent versions support 50-nsec cycle. Sequencer helps host computer download code into a RAM microprogram store (for accelerator applications). Fabricated in CMOS.

I—DATA-MANIPULATION INSTRUCTIONS
For ADSP-1101 16-bit integer arithmetic unit:
Add and subtract, multiply, multiply and accumulate (MAC).
Conditional multiply and accumulate.
Dual 40-bit accumulator control and internal feedback.
Logicals and shifts.
Block floating-point shifters and control.
For ADSP-321X/2X floating-point multipliers and ALUs:
Multiply single-precision floating point, double-precision floating point, and 32-bit fixed point.
Complete arithmetic and logical ALU operations.
Complete format-conversion operations.
II—DATA-MOVEMENT INSTRUCTIONS
For ADSP-1410 16-bit address generator:
Preupdate and postupdate mode conditional looping (zero overhead).
Add or subtract increments or offsets to pointers.
Register transfers.
Logicals and shifts.
Bit-reverse output (for FFT).
III & IV—PROGRAM-MANIPULATION AND -STATUS INSTR
For ADSP-1401, 16-bit program sequencers:
Jump and branch-absolute, relative and indirect.
Push, pop data, counters, and pointers to subroutine stacks.
Modify subroutine stack and register stack pointers.
Interrupt masking and control.
Writable control store (for downloading).

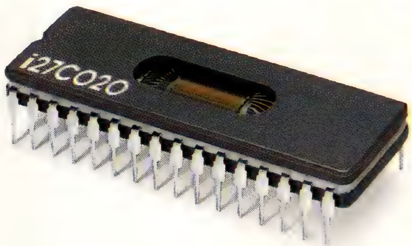
HARDWARE — SUPPORT — SOFTWARE

Supplier recommends same approach to development systems as that used with bit-slice microcoded components (ie, the AMD 2900 family). Suitable ROM-simulation systems are available from Step Engineering (Sunnyvale, CA) and HiLevel Technology (Tustin, CA). Similar aids are offered by Tektronix and Hewlett-Packard.

Mnemonics with microcode fields are available from the supplier for use with a meta-assembler. These programs can be used by a designer to create a design-dependent assembly-level language. Step Engineering, HiLevel Technology, and Microtek Research (Santa Clara, CA) meta-assemblers support parts via definition files for Word Slice mnemonics. Most of the parts are included in Logic Automation (Beaverton, OR) simulation libraries.

Now that we've been properly introduced,

take me home.



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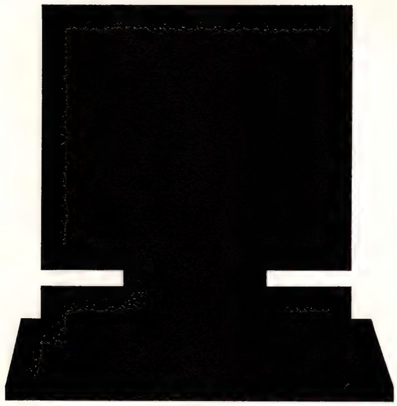

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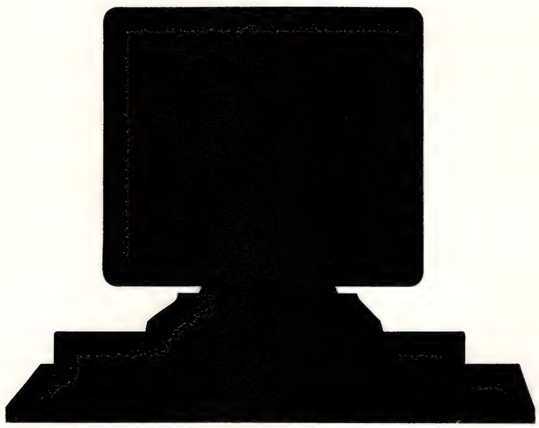

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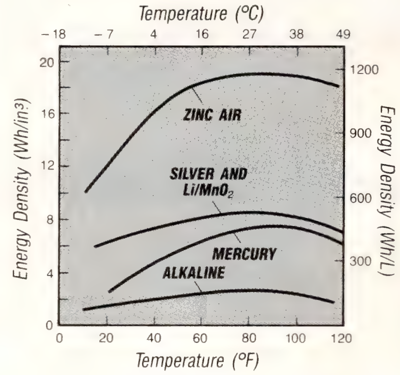

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Algorithm facilitates image recognition and position control

The correlation-function algorithm's simplicity makes it an oft-used tool for image recognition and an effective one for real-time image-position control.

Alexander Brengauz, *Consulting Engineer*

Advances in electronic-scanning devices, the advent of high-speed A/D converters, and the availability of large memories permit recognition analysis of stored image data. Consequently, image recognition is playing an increasingly important role in many position-control applications. An efficient image-recognition algorithm, such as the correlation function, can compare a scanned image pattern with a pattern stored in memory and subsequently control a device based on the scanned object's position.

An example of a typical image-recognition and position-control application is the position control of an imprinted image on a printing press's moving web. Each time the web rotates, a video scanner, which is located above the web, generates a waveform based on the sequence of imprinted images. Although the waveform appears random for a particular image, it is deterministic. An image-recognition system, with a copy of the deterministic waveform stored in an array, can use correlation techniques to identify the image's position.

Initially, the host must store a replica of the image waveform in memory, a process known as learning. During learning, an A/D converter samples the output of the scanner as it scans an imprinted image. A host µP stores each digitally converted sample in a reference array. The µP then calculates the sampled mean of the stored samples and subtracts it from each element in the array. The image-recognition system can now concatenate the stored elements in the reference array to generate a continuous reference pattern.

Once the learning process is complete, the system can then use correlation techniques to locate the position of the imprinted image on the rotating web. In one implementation, the system creates a new array from the imprinted images on each rotation. A µP subtracts the sampled mean from each element in the new array before correlating it with the data in the reference array. The system can now correlate the reference pattern with the data in the new array to locate the position of a particular image. The following steps illustrate one method you can use for correlation:

- Store a new-image pattern in a new-image array.
- Compute the mean for the new-image pattern.
- Normalize the data in the new-image array by subtracting the mean from each element in the array.
- Compute one of the correlation coefficients and store it in a function array.
- Advance (or set back) the address for the reference array to compute the next coefficient.
- Repeat the last two steps until the algorithm computes 2m coefficients.

The correlation technique offers certain advantages over FFT techniques. Generally, correlation algorithms are simpler; they don't require the 16-bit preci-

The correlation function for very similar patterns exhibits a positive maximum point, which represents the variance between the patterns.

sion mathematics of FFT algorithms. In fact, a correlation function with two bits of resolution is often sufficient for statistical analysis.

The correlation function consists of a number of coefficients computed as sum-of-products of elements in the new and reference arrays. The distance between each coefficient is a programmed offset in the address word that is used to access the elements in the reference array. The offset essentially shifts the elements of the reference array relative to the elements in the new array before summing the products of the elements. The correlator computes a correlation coefficient according to the formula

$$C_m = \sum_{n=1}^{N} P_n * R_n,$$

where C_m is the mth coefficient, N is the total number of the elements in the array, P_n is the nth element in the new array, and R_n is the nth element of the reference array shifted by the address offset.

The correlation function for very similar patterns exhibits a positive maximum point, which represents the variance between the patterns. In addition, similar patterns generate even correlation functions, which are highly symmetrical about the maximum point. The correlation function for dissimilar patterns is not necessarily a symmetrical function—a property that can be used to measure the degree of pattern resemblance.

In addition, the shape of the correlation function for a particular pattern is usually unique; it depends on the pattern's spectral composition. If you need information on the pattern's spectral distribution you can perform an FFT on the correlation function. Because most of the important spectral information for the correlation function lies in a narrow region of its waveform, it is faster to perform an FFT on the correlation function than it is to perform an FFT on the pattern's time waveform.

Fig 1 depicts the process for calculating the correlation functions for an image at two different positions on a press's web. An analog representation for two image patterns, whose positions differ by E, is shown in waveforms B and C, respectively. You compute the respective coefficients for each correlation function by first shifting the reference pattern and then multiplying the data in the reference array by the data in the new array. Waveforms D through H depict this operation.

The correlator accumulates all of the product terms for a particular offset to compute one of the coefficients. To calculate the complete correlation function, the data in the reference array must be concatenated to extend the reference pattern a minimum of $\pm$m in either direction. The resulting correlation functions for the two respective images are shown in waveforms I and J.

By locating the largest coefficient, you can determine the position of the image on the web. For the example shown in **Fig 1** the peaks of the correlation functions differ by E samples, which is proportional to the position difference between the two images on the web. Once you locate the largest coefficient, you can determine the degree of similarity between the reference pattern and the new pattern by comparing the sum of the coefficients to the right of the maximum to those to the left. When the patterns are very similar, the sums compare favorably.

To illustrate the use of correlation in a position-control application, consider a printing-press web with an image that repeats every 20 in. If you use N = 2048 samples to represent the image, you realize a position resolution of 20/2048≈0.01 in. between samples. Assuming that there is a 1-in. maximum uncertainty in

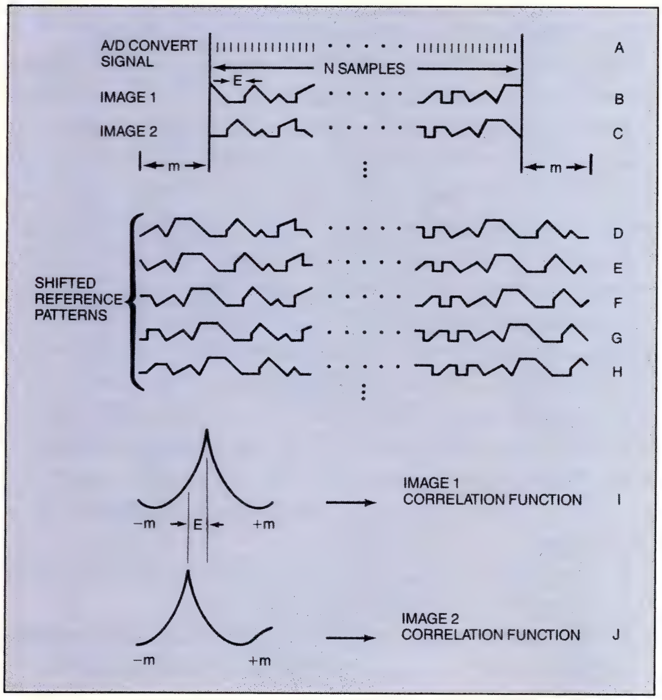

Fig 1—By accumulating the product terms obtained by multiplying a shifted reference pattern *with the new-image data, you can calculate each of the correlation coefficients. In this manner, the largest coefficient determines the relative position of the image on a printing press's web.*

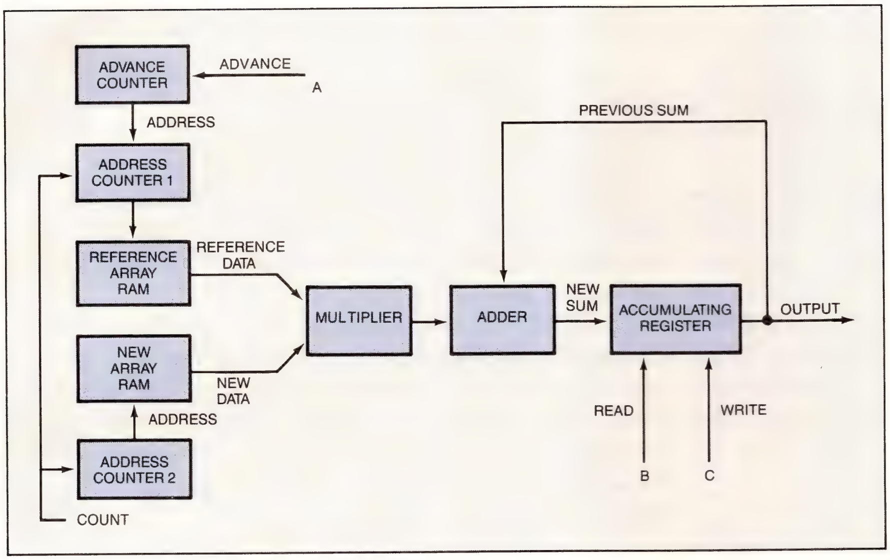

Fig 2—A dedicated pipeline correlator streamlines the tedious computation of the coefficients. *The correlator uses separate arrays for the normalized reference pattern and subsequent (new) patterns.*

the image's position, and that the sampler searches this uncertainty range with a 20% overlap, the total uncertainty in the image's position is 1.2 in. on either side of its nominal position—a total of 2.4 in.

Because each computed coefficent in the correlation function represents 0.01 in., the function must contain $(2048/20) \times 2.4 = 245$ coefficients to adequately cover the uncertainty range. In this example, therefore, the value for m in **Fig 1** is 122. (Actually, one side requires 123 coefficients, because the total number of coefficients is odd—245.)

A dedicated pipeline speeds computation

A dedicated pipeline correlator should perform the coefficient calculations, because the process itself requires a great deal of computation time and power. One of the many architectures for a dedicated correlator is shown in **Fig 2**. This pipeline correlator uses an overlapped instruction to perform the following operations:

- Fetch an element from the reference array addressed by counter 1 and an element from the new array addressed by counter 2 for multiplication.
- Fetch the contents of the accumulating register and the multiplication results for summation in the adder.
- Save the summation in the accumulating register.
- Increment the counters to initiate the next cycle.

The correlator must complete N instructions to calculate one of the coefficients when there are N elements in the new array. Assuming that the correlator can complete an instruction in 60 nsec and that $N = 2048$, it requires $60 \times 2048 = 122{,}880$ nsec to compute one coefficient. The total computation time for 245 coefficients is $122{,}880 \times 245 = 30.1$ msec.

However, in many instances a 30-msec computation time is too long. The pipeline-correlator architecture shown in **Fig 3** accelerates the computation time. This accelerated method relies on the fact that the mathematical mean for a stationary process is constant, implying that the arithmetic average for a particular image is also constant, whereas the average for different images is most likely variable. Because the samples for a particular image are assumed to be stationary, you can calculate the mean of the stored reference pattern and subtract it from each successive sample of the new pattern directly at the A/D converter's output.

The correlator multiplies the data that results after subtraction with each element in the reference array. Each multiplication term is destined for storage in a file of 2m accumulating registers. Before storage, however, the adder adds the accumulated sum in the mth register to the mth multiplication term to generate a running sum. Thus, the correlator calculates the correlation coefficients on the fly without the need for a new-pattern array.

To store data in the accumulating-registers file, the correlator shown in **Fig 3** increments counter 1 to fetch the mth element in the reference array for multiplication with the difference data and increments counter 2 to fetch the contents of the mth accumulating register and the multiplication results for summation in the

Often, a correlation function with two bits of resolution is sufficient for statistical analysis.

adder. It saves the summation in the mth accumulating register, and increments counter 1 to initiate the multiplication by the m + 1th element.

The correlator must cycle through all of these steps 245 times between each convert command to the A/D converter. Each convert command increments the convert counter and resets counters 1 and 2. This process continues until the A/D converter converts the entire 2048 samples for the image. Next, the correlator reads the 2m coefficients from the register file and resets the convert counter to prepare to process the next image.

Accelerated method is a real-time saver

Because the number of stages in the pipeline for the accelerated correlator is the same as that in the new-array correlator, it is reasonable to assume that you can accomplish an instruction in the same time period—60 nsec. Under this assumption, the correlator can calculate 245 terms in $60 \times 245 = 14{,}700$ nsec. Therefore, the accelerated method calculates the entire 245 coefficients for the correlation function in 0.0147 msec after the correlator converts the 2048th sample for a new image—a considerable speed improvement over the 30.1 msec necessary to calculate the coefficients when using a new-pattern array.

Because the minimum time between consecutive samples is 14,700 nsec, and the number of samples is 2048, the total time required to enter all of the data for the coefficients is $14{,}700 \times 2048 = 30.1$ msec—the same time it takes using the new-pattern array method. Therefore, both techniques require that the linear speed of a web with the reference image imprinted every 20 in. is less than $20/30.1 = 0.664$ in./sec, or approximately 3300 ft/min.

However, the accelerated method allows you to terminate the process before using all of the 2048 samples to the calculate the coefficients. Because dropping several of the last samples has a small effect on the overall computation accuracy, the method allows the web to operate at a faster linear speed than it could using the new-pattern array approach. EDN

Author's biography

Alexander Brengauz is a consulting engineer. Prior to consulting, he was employed by Quad/Tech in Pewaukee, WI. He holds an MSCS from the Institute of Electronics and Automation in Moscow, USSR, and an MSEE from the Institute of Mechanization in the USSR. He holds two patents, one from the United States and one from Europe. In his spare time he enjoys skiing and sailing.

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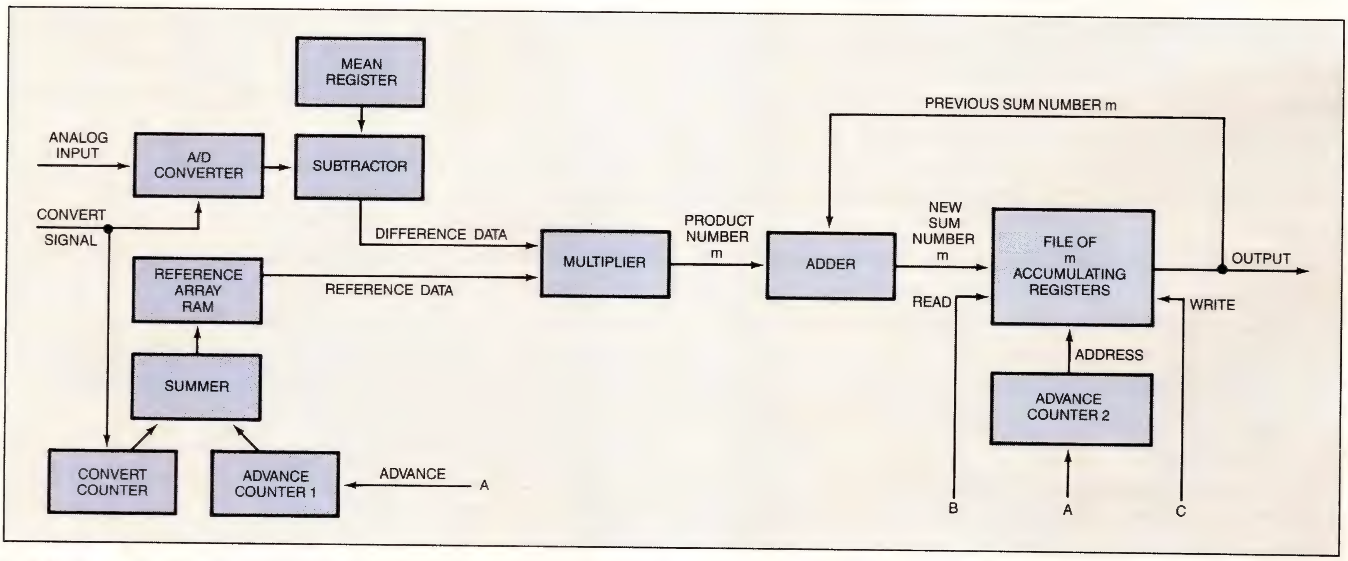
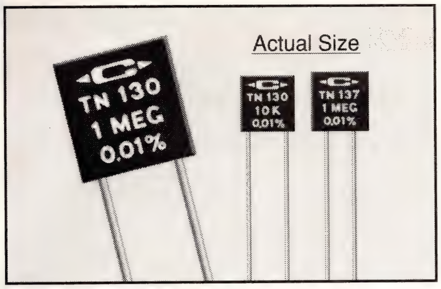


Fig 3—An accelerated correlator, *based on the stationarity of the samples, subtracts the mean from the samples at the A/D converter output. The correlator calculates running sums for the coefficients and accumulates the sums in a file of registers.*

Type TN Lab Grade Low TC Precision Resistors

New



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Low TC to 5 ppm/°C, 0°C to 70°C

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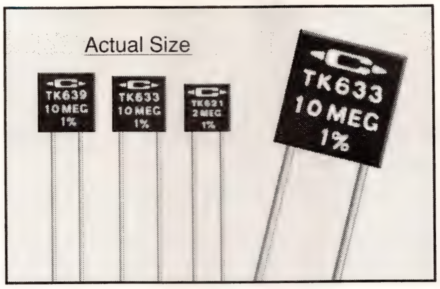
Type TK Low TC Precision Radial-Lead Film Resistors



Low TC to 5 ppm/°C, -55°C to 125°C

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- TC of 5, 10 or 20 ppm/°C, -55 to 125°C
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- Space Efficient Radial-Lead Design

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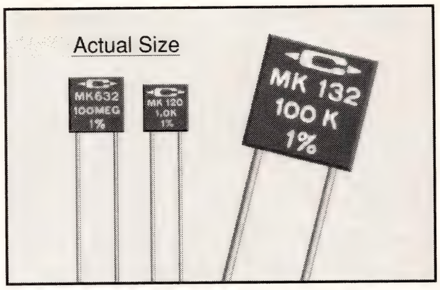
Type MK Precision Power Radial-Lead Film Resistors



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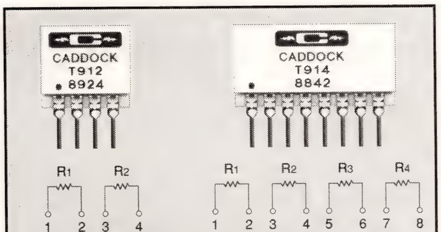

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T914 Schematic
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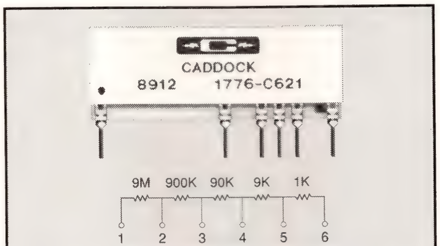

1776-C621 Schematic

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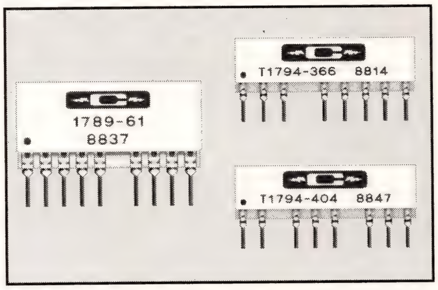

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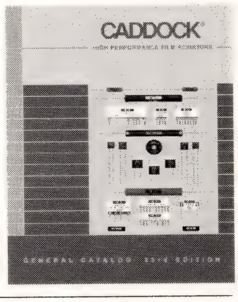

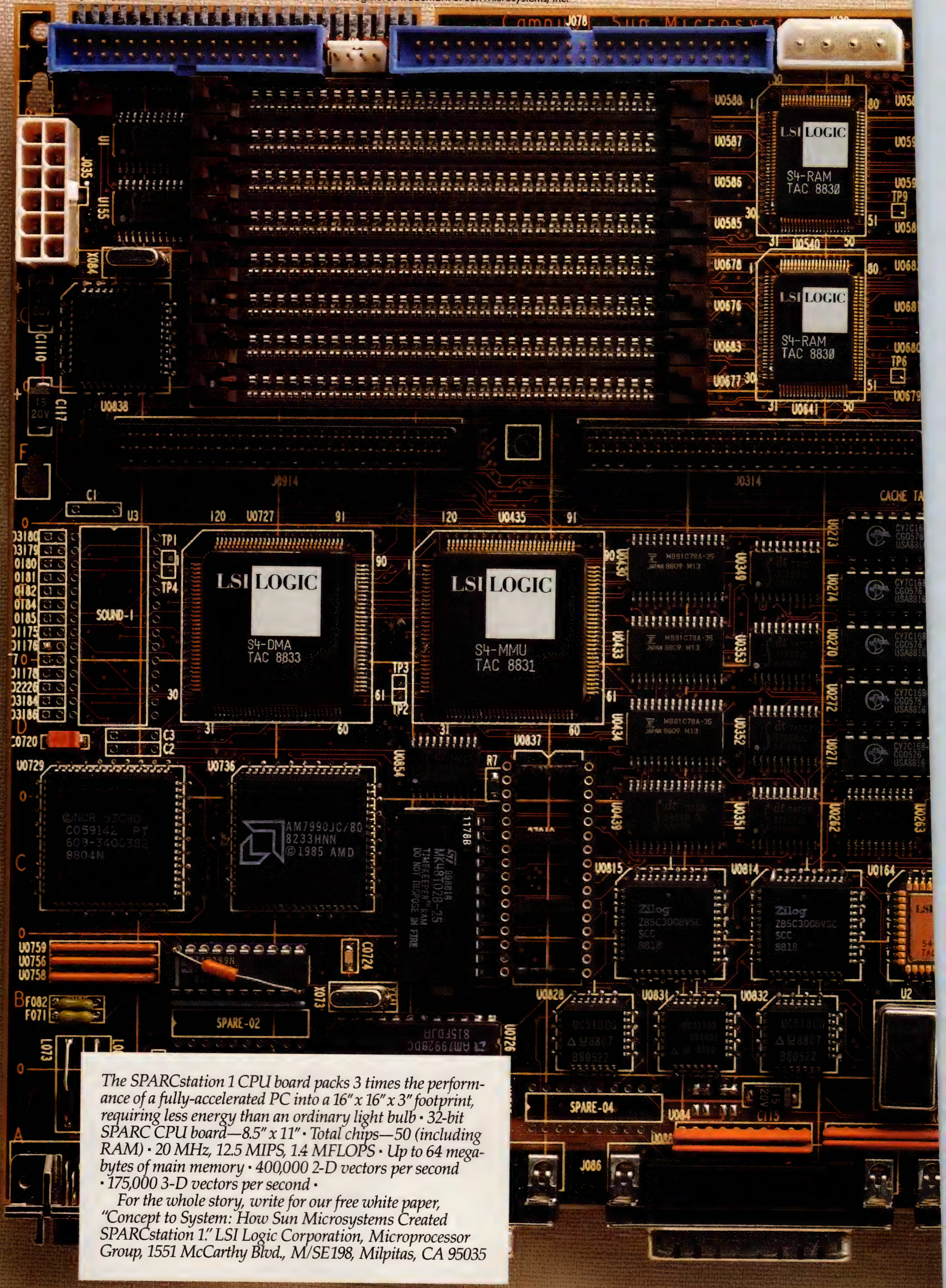
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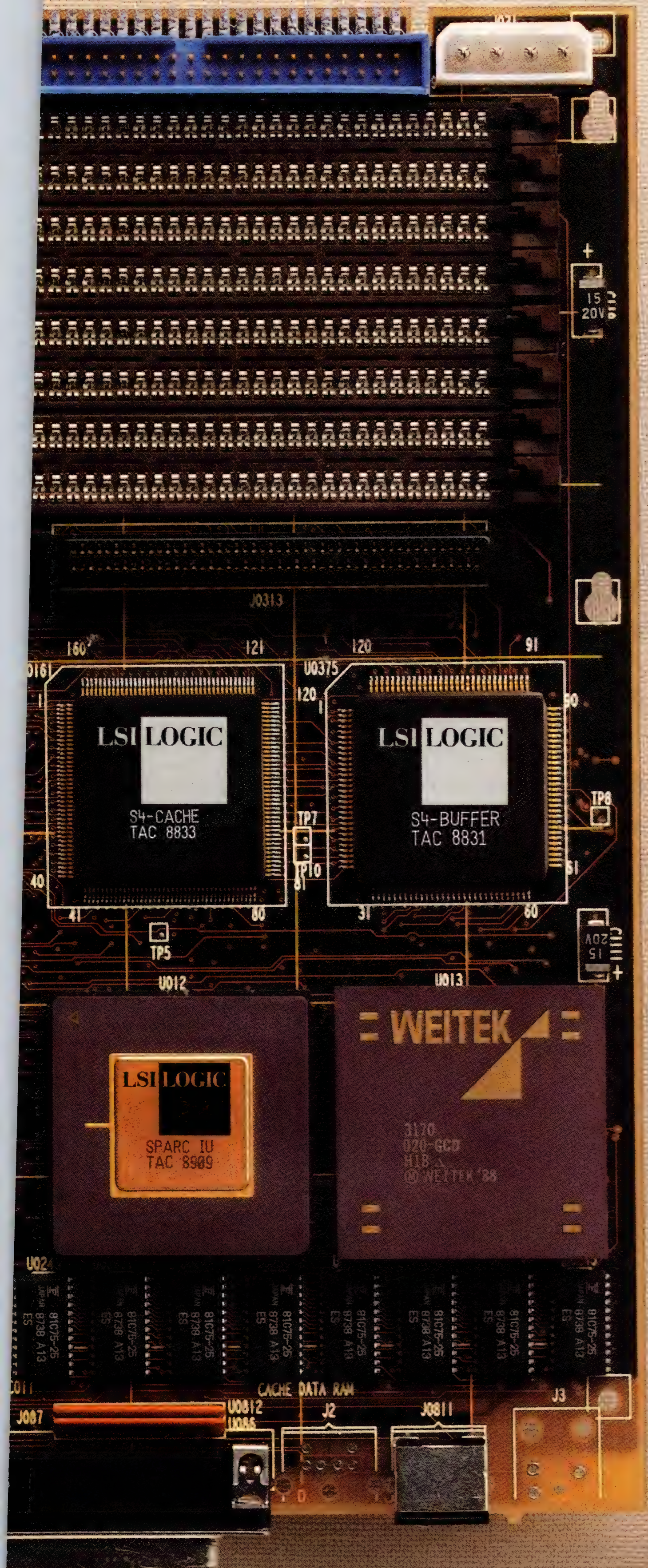

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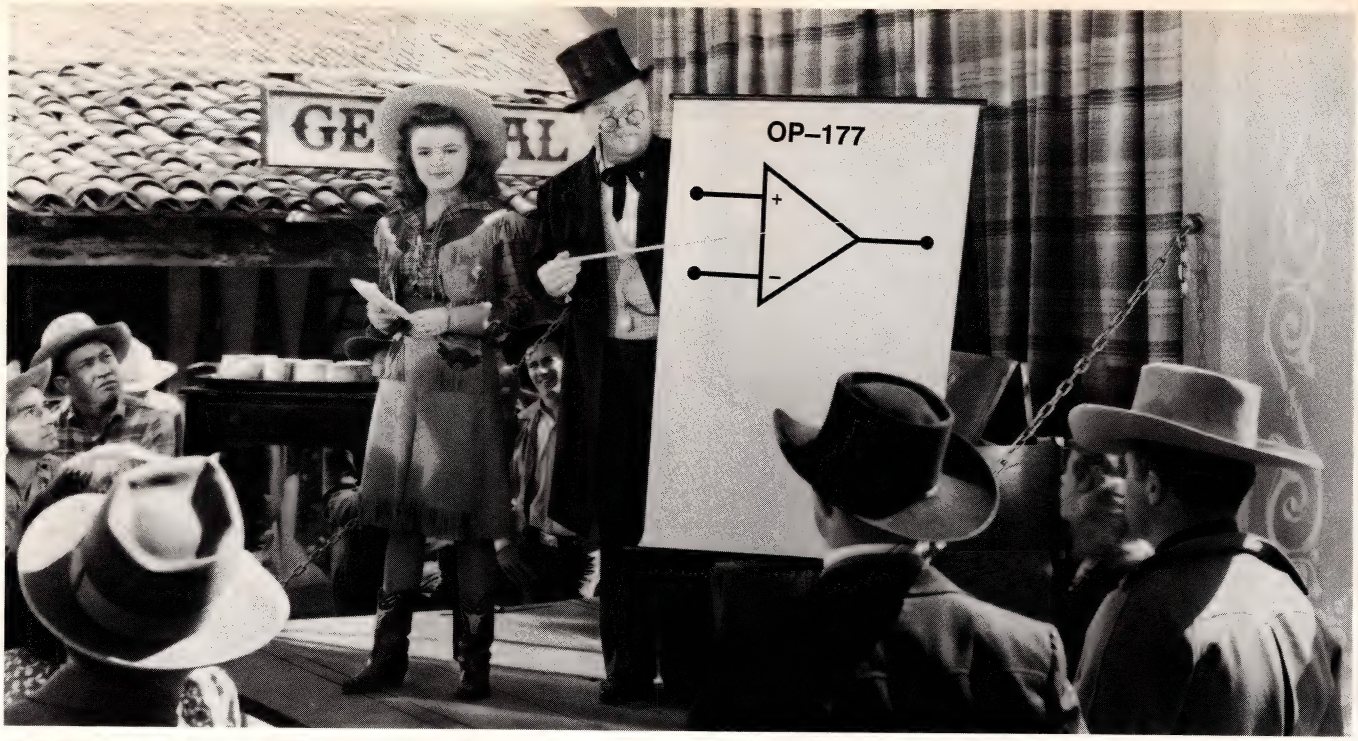

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CIRCLE NO 86

DESIGNER'S GUIDE

Fine-tuning
μP/μC code
Part 2

Resonant converters team control theory and circuit design

Part II of this 2-part article on resonant-mode power-supply design techniques outlines the control-loop, output-filter, and transformer designs. By choosing components and safety margins so that your design satisfies all the requirements of zero-current or zero-voltage switching, and by paying attention to fault-control and start-up considerations, you can attain the benefits of the resonant-mode technique.

Frederick E Sykes, *Gennum Corp*

Although the block diagrams of quasiresonant-mode power supplies and the more familiar PWM power supplies are quite similar, both major and minor circuit differences exist that you must consider when designing the control loop and other support circuits. The control loop is a critical component of any power-supply design and greatly affects the supply's final specifications. These specifications include the load regulation, line regulation, load transient response, and stability of the output under all load and line conditions.

As with any design, you should quantify your resonant-mode supply's specification goals before you begin its design. To illustrate a detailed resonant-mode design, **Fig 1**, a very popular quasiresonant converter topology, shows a more detailed schematic of the off-line power supply used as an example in Part I. The target specifications of this half-bridge-configured supply are

- nominal input voltage: 110V ac
- output voltage: 5V at 25A
- minimum output current: 0.9A
- efficiency: approximately 80%
- maximum output ripple: 100 mV p-p
- line regulation: better than ±0.5% for inputs between 95 and 132V ac
- transient response: output settles to within ±5% in 500 μsec for a 50 to 100% step load.

In addition to these specifications, you also must choose the desired switching-frequency range. The fundamental requirement of quasiresonant converter designs—zero-current or zero-voltage switching—is that the switching frequency be lower than the resonant-tank frequency. This timing relationship ensures that a dead time will exist between cycles. The practical frequency limit of zero-current-switching resonant converters is approximately 1 MHz. At higher frequencies, you may have problems with the ferrite material currently available for resonant-mode designs. In the present example, the design goal for the resonant tank's frequency is 750 kHz.

To determine the maximum allowable switching frequency, you must establish timing relationships between the resonant and switching frequencies at both

To ensure lossless switching, the resonant frequency must be at least 20% higher than the switching frequency.

nominal and worst-case conditions. Under no-load conditions, the resonant tank's current and voltage waveforms look like **Fig 2a**; note that I_{LR}'s waveform is centered around zero. Under maximum-load conditions, the waveform looks like **Fig 2b**; note that here I_{LR} barely goes negative.

To guarantee zero-current switching under all line and load conditions, the current must reverse direction—go negative—for some period of time. Remember that the term "zero current" doesn't imply "zero crossover" switching. As long as the resonant inductor's current is negative, the switch carries "zero current" because the negative current flows through D_3 and D_4. You should design for a negative-current time that's equal to 25% of the full cycle under nominal conditions. You'll want the FET's drive pulse to turn off at the midpoint of this negative-current cycle, or at 87% of the resonant cycle's period. Thus, the desired on time for the switches in this design is 1160 nsec. **Fig 3** summarizes these timing relationships.

Unfortunately, tolerance variations in the resonant inductor and capacitor will always exist. The errors in inductor and capacitor values affect the tank's characteristic frequency in addition to the energy in the tank. If these variations shift the resonant frequency by too much, another resonant cycle may begin before the previous one has ended. If overlap occurs, the circuit operates in the continuous-resonance mode, and this mode's nonzero-current switching entails higher switching losses.

To ensure that the gate's drive pulse can't start another cycle unless the previous one is complete, add a 20% difference between the resonant frequency and the switching frequency. With this added margin, the controller's switching period will equal the resonant period plus 20%, or 1600 nsec. Thus, the controller's commutation frequency is approximately 600 kHz. Including a certain amount of dead time in your design

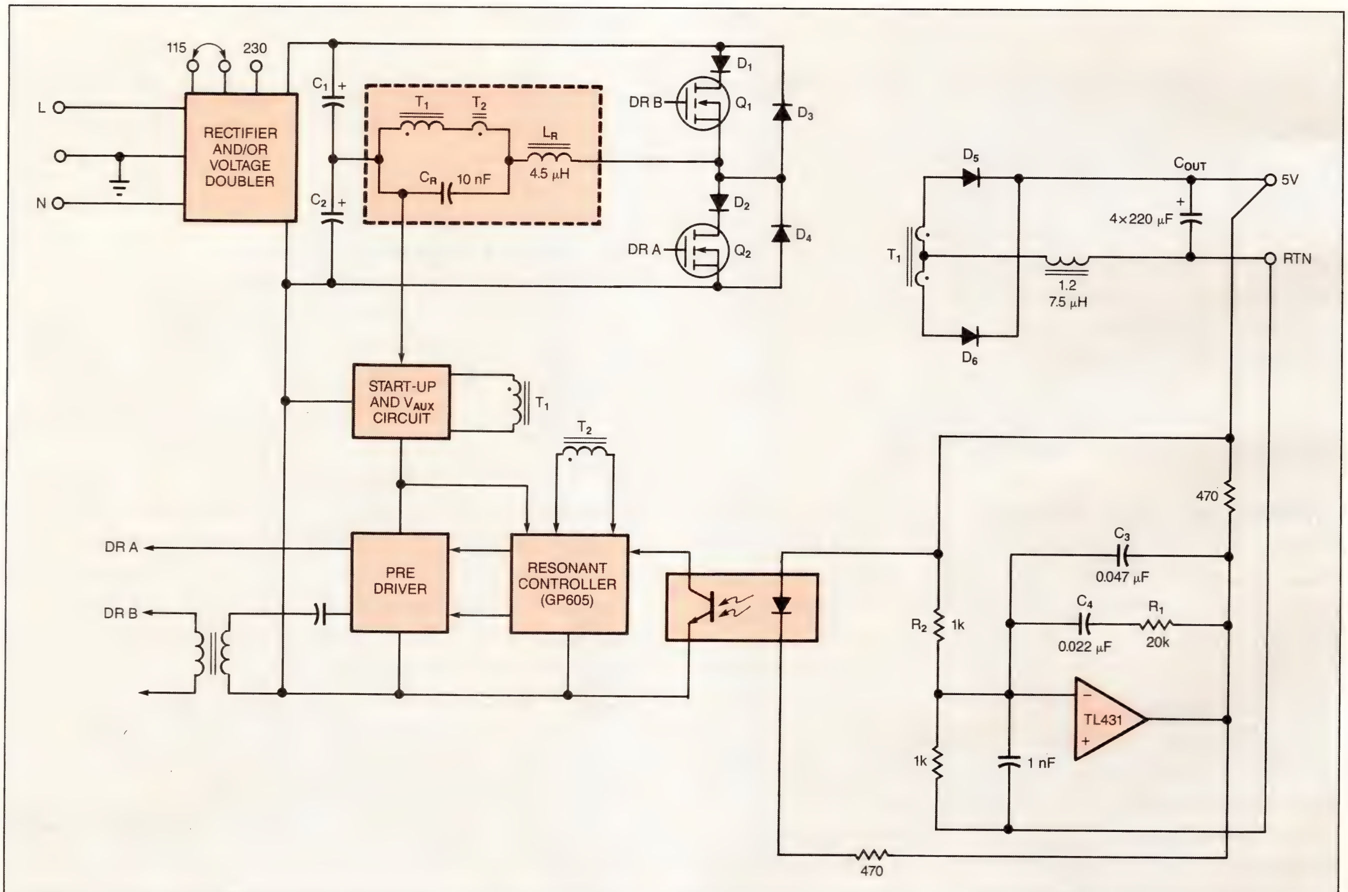

*Fig 1—**Switches Q_1 and Q_2** in this 5V, resonant-mode power supply alternately apply half of the rectified voltage to the resonant tank, L_R and C_R. The ultrafast recovery diodes, D_3 and D_4, conduct the reverse current.*

also ensures that the resonant capacitor is completely discharged at the beginning of each cycle.

Once you know all your target specifications, you can choose specific component values for the circuit blocks of your quasiresonant-mode supply. **Fig** 4's block diagram is representative of all off-line supplies. One main difference between quasiresonant-mode designs and more common PWM designs is the type of control. Most resonant-mode controllers implement a voltage-to-frequency conversion as opposed to the voltage-to-duty cycle conversion of PWM controllers.

Output filter is central to performance

One of the central elements of **Fig 4**'s block diagram is the output filter because it largely determines the power supply's frequency and ripple characteristics. In general, if the output filter's cutoff frequency is lower than the switching frequency, no high-frequency signals will corrupt the supply's output. As required in PWM designs, you must design the output filter so that the supply meets its output-ripple specification. In PWM supplies, the choke's ripple current is triangular, whereas in resonant converters the output current is sinusoidal because of the sinusoidal voltage on the secondary. The resonant converter's transformer secondary voltage is

$$V_{SEC}(1-\mathrm{COS}\ 2\pi t/T_R)$$

where V_{SEC} is the peak dc voltage on the secondary, and T_R is the resonant period. The output inductor's voltage, therefore, is

$$V_{SEC}(1-\mathrm{COS}\ 2\pi t/T_R)-(V_{OUT}+V_F)$$

during the resonant period. V_F equals the forward voltage drop of the output diodes, D_5 and D_6. When high currents flow through these diodes, V_F can be as high as 1V.

The worst-case ripple of resonant-mode designs occurs under the same conditions as in PWM designs but for slightly different reasons. The worst case for PWM designs is high-line and maximum-load conditions, because the duty cycle is low, and the output capacitor

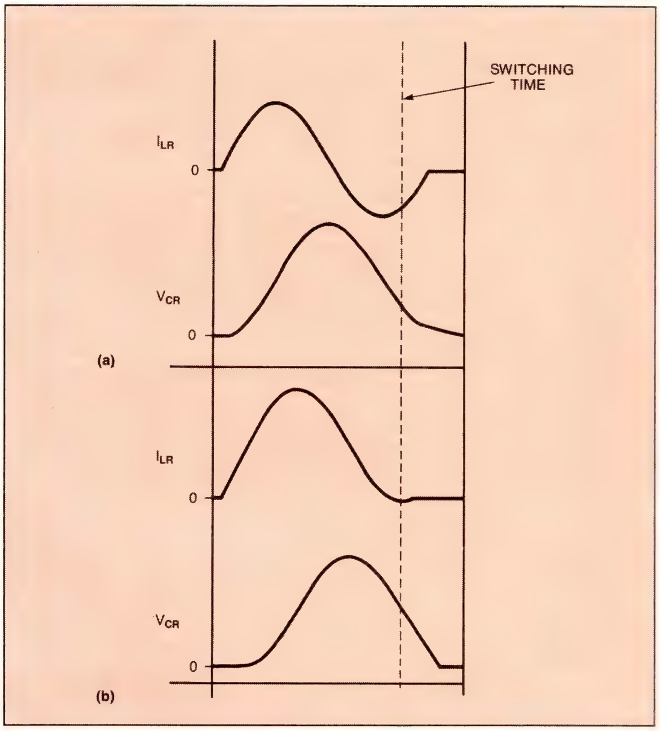

***Fig 2—At low load current,** the charge remaining on the resonant capacitor is small, but the capacitor's discharge time is long **(a)**. At high load current, the remaining charge is large (almost one-half the line voltage), but the high load discharges the capacitor rapidly to allow high-frequency operation **(b)**.*

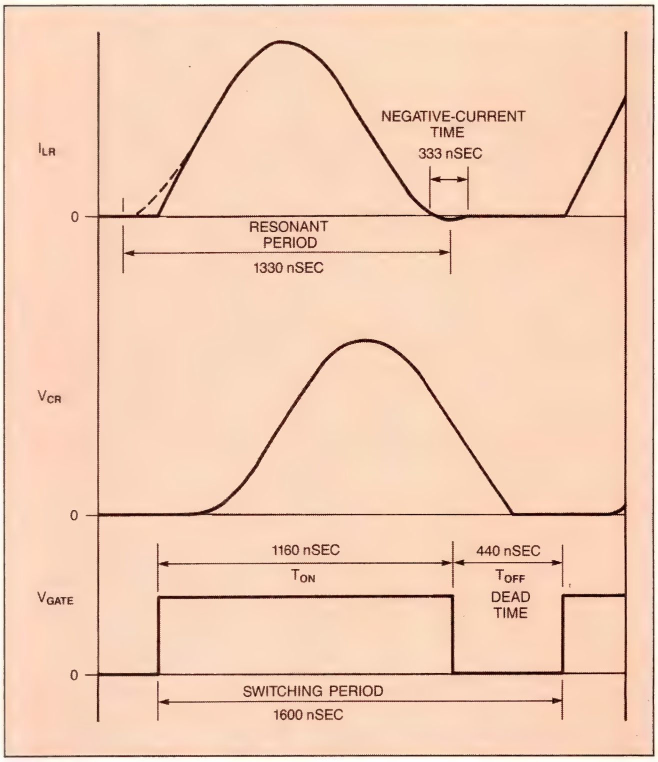

***Fig 3—To ensure zero-current switching under all conditions** including worst case (maximum load with low line input), this design includes a 25% dead time (440 nsec) and at least 333 nsec of reverse-current time.*

One of the central elements of a resonant-mode design is the output filter, because it largely determines a supply's output-ripple characteristics.

is discharging at its maximum rate. For resonant-mode designs, the worst-case ripple is also at high line and maximum load, because the switching frequency is low, and the rate of capacitor discharge is at a maximum.

The output-inductor current is approximately

$$I_L(t) = \int \frac{1}{L} [V_{SEC} - V_{SEC} \cos 2\pi t/T_R - (V_{OUT} + V_F)] Dt$$

When you integrate equation 4 over the entire resonant period, the result is

$$IL_{PEAK} = \frac{T_R}{L} [V_{SEC} - (V_{OUT} + V_F)]$$

IL_{PEAK} is the peak ac current in the inductor. The dc current equals the output-load current. The turns ratio and the maximum input line voltage determine the value of the peak secondary voltage, V_{SEC}, as follows:

$$V_{SEC} = \frac{\sqrt{2}\, V_{LINE}}{\text{TURNS RATIO}}$$

For this design example, the high line is 132V rms, and the turns ratio is 12:1. Thus, the peak voltage on the transformer secondary is 16V. Choose the output inductor's value so that the inductor just barely conducts at the minimum load of the power supply. A rule of thumb is that IL_{PEAK} should equal at least $2 \times I_{OUTMIN}$. For this design, therefore, $IL_{PEAK} = 1.8A$. Using the above equation for IL_{PEAK}, you can solve for the minimum value of L. For this particular design, V=16V, $V_{OUT} = 5V$, $V_F = 0.7V$, and $T_R = 1330$ nsec. Thus, the minimum L is 7.5 μH.

You can use several approaches to find the minimum value of the output capacitor. One approach is to take the integral of the positive half cycle of the capacitor current to find the maximum charge—hence the maximum ripple—on the capacitor. This approach yields a vastly underestimated value for C_{OUT}, because it neglects the capacitor's equivalent series resistance. In most designs, the equivalent series resistance is the dominant factor that affects the capacitor's value. The effects of this resistance usually cause the required C to be approximately 10 times greater than the value you'd get using the integral approach. The maximum allowable equivalent series resistance is V_{RIPPLE}/IL_{PEAK}, which is 100 mV/1.8A or 55 mΩ for this design. To meet this requirement, the design requires four 220-μF, military-grade, low-equivalent-series-resistance capacitors connected in parallel, which reduces their combined equivalent series resistance.

Another important block in **Fig 4** is the error amplifier. Resonant-mode designs commonly use voltage feedback rather than current feedback. The conventional current-mode control used in PWM supplies isn't applicable to resonant mode (**Ref 2**), because it depends on the existence of a current ramp through the trans-

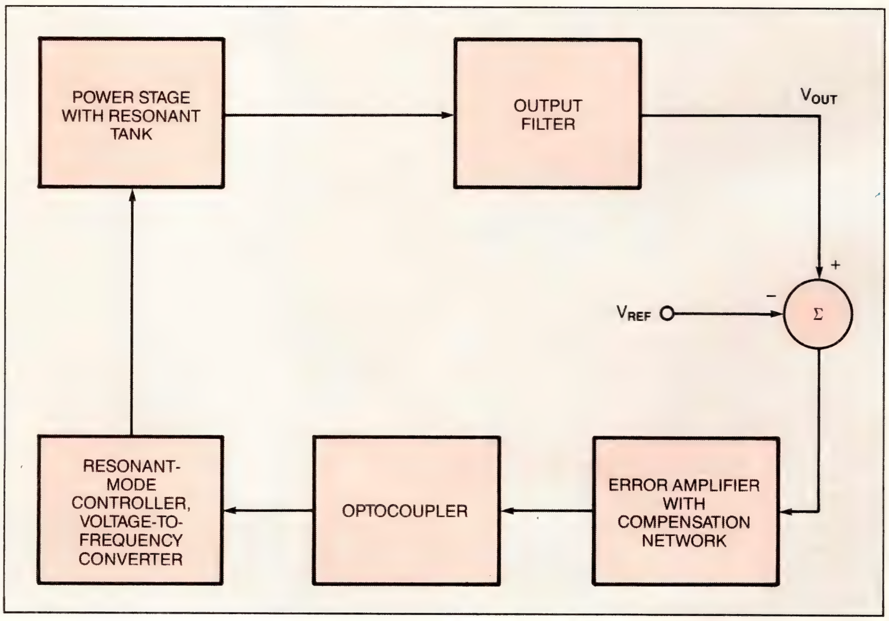

***Fig 4—A resonant-mode power supply's control loop** contains the same functional blocks as do PWM supplies with one exception: a voltage-to-frequency converter replaces PWM's voltage-to-pulse-width converter.*

The control loop of resonant designs uses voltage feedback rather than current feedback because the latter requires square-wave transformer signals.

former. This current ramp occurs only if you apply a square-wave voltage to the transformer.

The feedback amplifier generates an error signal by resistively dividing the output and comparing the divider's output to a reference. This error amplifier, which uses the TL431CLP shunt regulator, also provides loop compensation. The transfer function of the amplification stage is

$$\frac{V_{OUT}(s)}{V_{IN}(s)}=\frac{s+1/R_1C_4}{sR_2C_3\left(s+\dfrac{C_3+C_4}{R_1C_3C_4}\right)}$$

C_3 is responsible for the first pole at 0 Hz, and it acts as an integrator to provide high dc gain for good dc regulation. The second pole is located at

$$f_2=\frac{C_3+C_4}{2\pi R_1C_3C_4}\text{ Hz}$$

and a zero is present at

$$\frac{1}{2\pi R_1C_4}\text{ Hz}$$

To avoid dc coupling, the output of the error amplifier drives an optocoupler that provides the necessary isolation between the transformer's primary and secondary sides. As with PWM designs, you can select the error-amplifier components and optocoupler gain to achieve the desired crossover point in the closed-loop response. The closed-loop crossover frequency for the overall control loop is 10 kHz; the phase margin varies between 47 and 94°, depending on line and load conditions.

As **Fig 4** shows, the optocoupler's output signal is the control voltage for the internal VCO of the resonant controller (GP605). The optocoupler and the controller each feature high gain, so they control the overall loop gain. The control IC's VCO generates a square wave at the operating frequency determined by the input signal. The controller divides the VCO signal into complementary phases (**Fig 5**). Then, the IC's internal monostable starts a fixed, on-time pulse at each edge of the main VCO square wave. The complementary square waves alternately gate this pulse to output A and output B. The controller accepts a voltage input and outputs a frequency. Thus, its gain is measured in Hz/V. The gain of the GP605 is linear between the minimum and maximum VCO frequencies. At the VCO's end points the frequency is clamped, and the gain drops to zero.

A restriction unique to resonant-mode designs because of the required zero-current switching is that the on time of the FET switch must be fixed. In zero-voltage switching, the off time is fixed. Most resonant-mode designs don't require this pulse width to be precise. For zero-current switching to occur, the controller can turn off the FET at any time during the negative-current cycle.

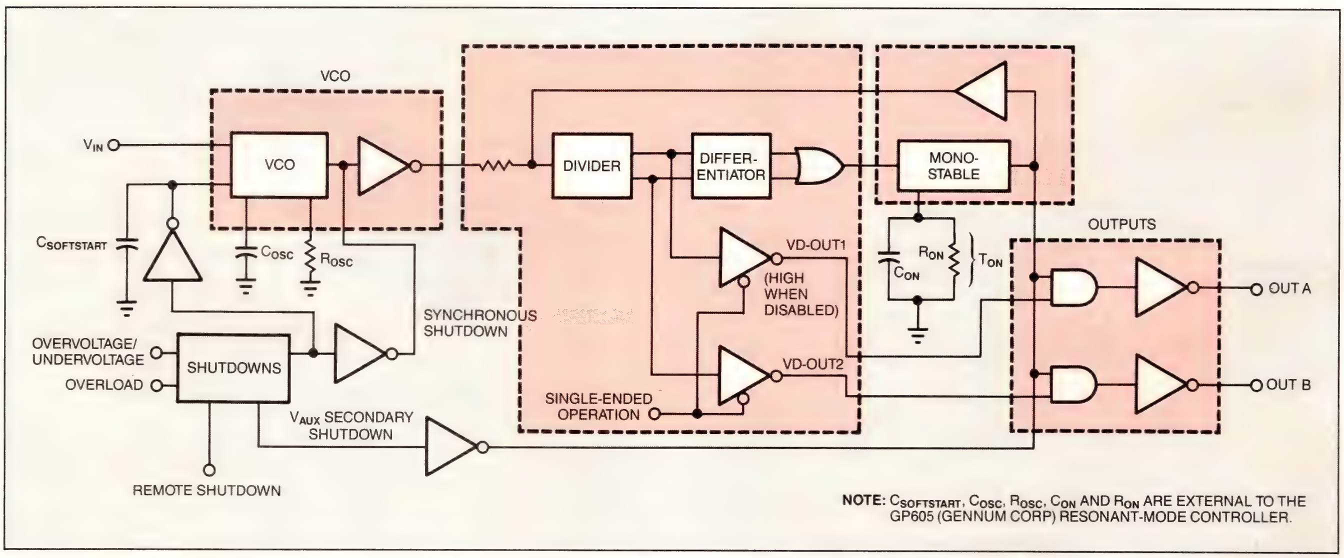

Fig 5—The resonant-mode controller IC *(the GP605 from Gennum Corp) responds to voltage inputs and delivers a fixed-width pulse. The supply's output regulation occurs as the chip varies the frequency of this pulse based on the voltage feedback.*

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The components of the resonant tank simultaneously must provide enough energy to the output tank and limit the current through the FET switches.

Because the control IC's output pulses are fixed, the controller can't react to variations in line or load once the pulse is triggered. Instead, the controller compensates for changes in output conditions by varying the start of the next pulse. This characteristic adds inherent phase delay to the feedback loop. The added phase shift equals 360° at the switching frequency. The switching frequency is always much higher than the loop bandwidth, so you can safely ignore the effect of this additional phase shift.

The GP605 controller generates high-current output pulses with a peak-current capability of about 800 mA using a totem-pole design. Usually this output current isn't enough to drive power MOSFETs directly unless the application requires less than 50W of power or a low input voltage. The current drive requirements of the FETs are very large because of the Miller multiplication of their gate-to-drain capacitances. As **Fig 1** shows, you can solve this problem by adding a predriver between the controller outputs and the power-FET inputs.

Resonant-tank design requires a balancing act

When you design the resonant tank—that is, when you choose the resonant inductor and capacitor values—you must fulfill two opposing requirements. First, enough energy must cycle in the tank to let the supply meet the load's energy demands. Second, your design must minimize the peak-current stress of the FET switches. The worst case for simultaneously fulfilling both of these requirements exists under low-line and full-load conditions. The energy stored in the tank equals

$$\frac{C_R V_{PEAK}^2}{2}$$

where V_{PEAK} is the peak voltage across the tank capacitor.

At the maximum frequency, the power in the tank is

$$P_{TANK}=\frac{C_R V_{PEAK}^2 F_{MAX}}{2}.$$

Losses occur during energy transfer from the tank to the output; $P_{OUT}=P_{TANK}\times\eta$, where η is the efficiency. For this design, the absolute minimum input voltage—the input at which the tank is barely supplying power to the load—is 78V rms. Because of the voltage doubler on the input, the dc voltage applied across the entire tank is $2\times\sqrt{2}\times 78$, or 220V. By using $V_{PEAK}=220V$, $P_{OUT}=125W$, efficiency=80%, and $F_{MAX}=600$ kHz, you can solve the above equation to find $C_R=10$ nF. You can then use the following equation to choose L_R so that the resonant frequency is 750 kHz:

$$L_R=\frac{1}{C_R 4\pi^2 F_R^2}.$$

For this example, L_R equals 4.5 μH.

The resonant transformer is different from a PWM transformer in that the applied voltage is a haversine wave and not a square wave. A haversine wave is a sine wave dc shifted so that its positive peak is at 2V, and its negative peak is at 0V (**Ref 4**). When calculating the turns ratio, account for this difference by using the average voltage of the haversine wave. The fact that the applied voltage is sinusoidal also affects the maximum operating flux density. The flux density in the transfomer equals

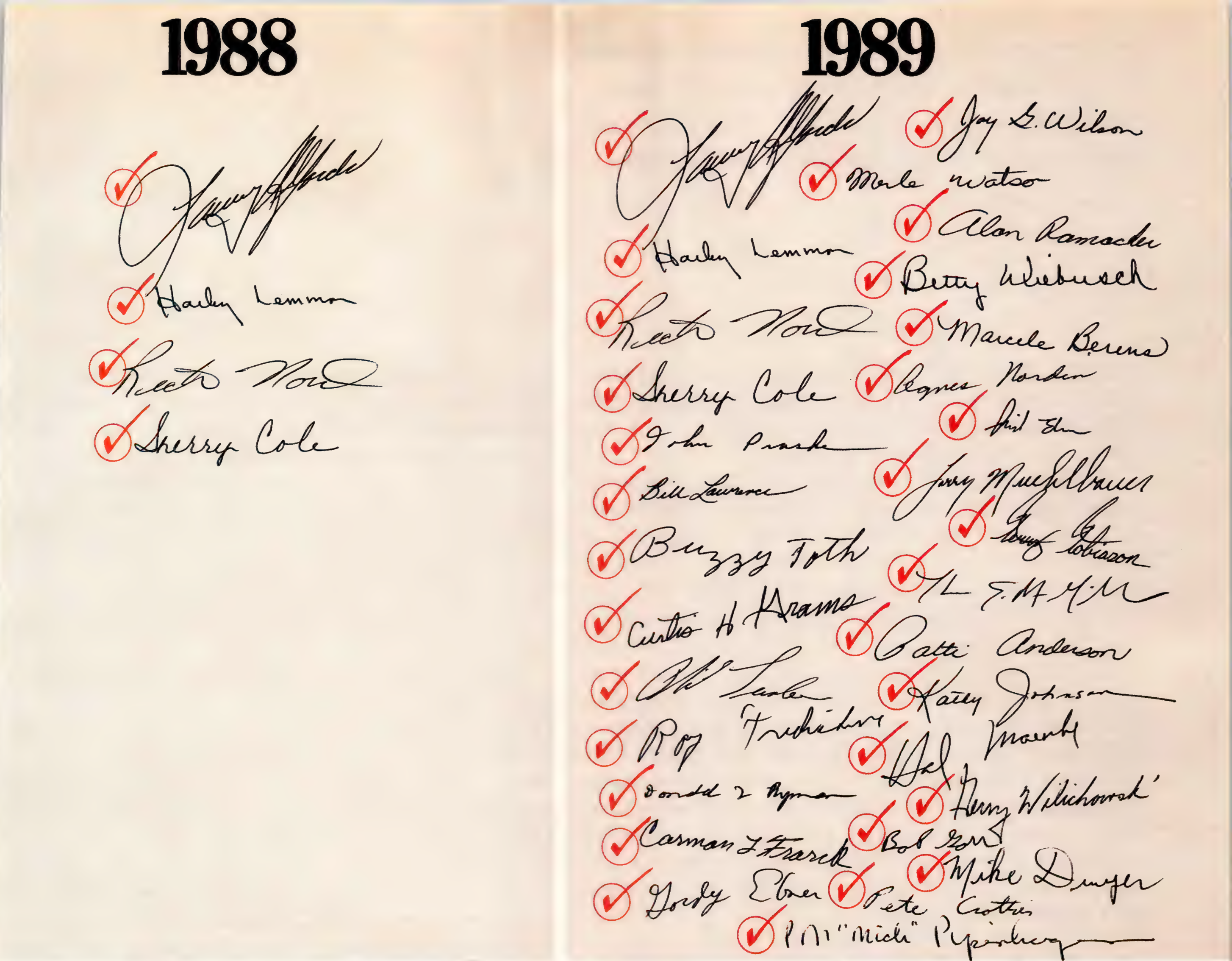
$$B_{MAX}=\frac{10^8}{NA_e}\int_0^{T_R} V_{PRI}\,Dt \text{ GAUSS}$$

where V_{PRI}, the primary voltage, equals $V(1\text{-}\cos 2\pi t/T_R)$; T_R is the resonant period; N is the number of turns on the primary; A_e is the transformer core area in square centimeters; and V is the maximum voltage applied across the resonant tank, or $\sqrt{2}\times V_{LINE}$. When you evaluate it over one complete cycle, this equation simplifies to

$$B_{MAX}=\frac{10^8 V T_R}{NA_e}\text{ GAUSS.}$$

Use this equation to calculate the core losses for your transformer design, and then check with the core manufacturer to ensure that the core losses are reasonable. Note that in this half-bridge example, the frequency applied to the core is approximately 300 kHz.

As long as the core isn't saturated, the high-frequency core losses result from hysteresis, residual, and eddy-current losses. Hysteresis losses are proportional to the maximum flux density times the frequency. Therefore, to increase the operating frequency from 10 kHz to 1 MHz, you'd have to divide the flux density by 100. Eddy currents are proportional to the square of the frequency, and thus at high frequencies, these currents cause a dramatic increase in losses. You can



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minimize losses by maximizing the ac core resistance, but this task usually requires special materials. The H7F material recently introduced by TDK is an efficient, high-frequency core material.

When designing the windings of a high-frequency transformer, you also must consider the skin effect. Normally, you'll want the secondary to have only a single turn. To minimize the skin effect, use copper foil for the secondary winding; either bifilar windings or copper foil is acceptable for the primary winding. Flat winding material is easier to work with if you etch the winding on a pc board, and then insert it onto the center leg of an E-core. This technique maximizes the utilization of copper, because the pc board's copper thickness is usually about twice the skin depth. This technique also minimizes fringing effects and leakage inductance because the windings are much wider than they are thick, and the thin profile allows very close coupling between the windings. Sandwiching the primary around the secondary also minimizes the leakage and improves the coupling.

Start-up and shutdown require open-loop stability

Although most of the circuit elements that correspond to **Fig 4**'s block diagram fulfill the control loop's closed-loop requirements, the open-loop stability of a power supply is also very important. Open-loop characteristics are especially critical when, for whatever reason, the feedback-voltage signal representing the error voltage lies outside the small-signal input range of the controller. The open-loop situation occurs at start-up and under fault conditions. Under these circumstances, a limit on the maximum frequency of the switch's drive waveforms is necessary. As long as the pulse width is still fixed, and you have control over the frequency, the operation of the supply will be predictable.

At start-up, the error amplifier drives the control IC to output its maximum frequency to deliver maximum power to the load, even if the load is close to its minimum. This power demand can put severe and unnecessary stress on the resonant tank, output transformer, and output filter. Also, the high-energy delivery will cause the output voltage to overshoot, which may cause oscillation. To eliminate these start-up problems, a soft-start feature is necessary. A soft-start circuit ensures that the control frequency always starts at the minimum frequency and ramps up slowly to the stable operating frequency, independent of the load. The GP605 controller performs this feature automatically on each start-up. Once the controller reaches its operating point, the soft-start circuit no longer limits the rate of change of the controller's output frequency.

A good soft-start-duration range is 30 to 48 msec. This amount of time gives the input capacitors, C_1 and C_2, several cycles to charge up before they must withstand the load's demands. High-power supplies—those with outputs greater than 500W—require a longer capacitor-charging time. In these cases, you may need soft-start times of 100 to 200 msec.

Protection under fault conditions is an area you must never neglect when designing a power-supply circuit. The basic conditions you must protect against are overvoltage, undervoltage, overload shutdowns, and the "hiccup" and soft-start delays. In addition, resonant-mode designs have a unique restriction not present in PWM designs: if a fault occurs during the on time of the FET when high sinusoidal currents are flowing, the FET must be able to complete its pulse to turn off at a zero-current point. The resonant switch can handle zero-current switching, but it probably can't handle the high power dissipation associated with a repetitive high-current turnoff. In the present example, the controller has a synchronous shutdown feature to prevent this problem. Once started, the drive pulse always completes a full cycle.

The combined voltage ratings of the FETs, diodes, and capacitors determine the overvoltage level. In **Fig 1**'s half-bridge circuit, the component stresses are never far above the maximum line voltage. In other single-ended, resonant topologies—such as the forward converter—the voltage can be as high as twice the line voltage. An appropriate overvoltage level provides the devices with a safety margin of 40 to 60V just before the overvoltage shutdown activates.

Set the undervoltage limit to ensure that enough voltage on the resonant transformer's secondary exists to regulate the output under minimum line conditions. Because an undervoltage or overvoltage condition shuts down the supply, restarting the supply requires a soft start. The controller also performs this function.

To avoid damage to the supply, your design must also handle output overloads caused by short circuits. To accomplish this task, resonant-mode and PWM supplies use the same technique: a current-sense transformer senses the current flowing through both the power transformer and the switch. The sense winding

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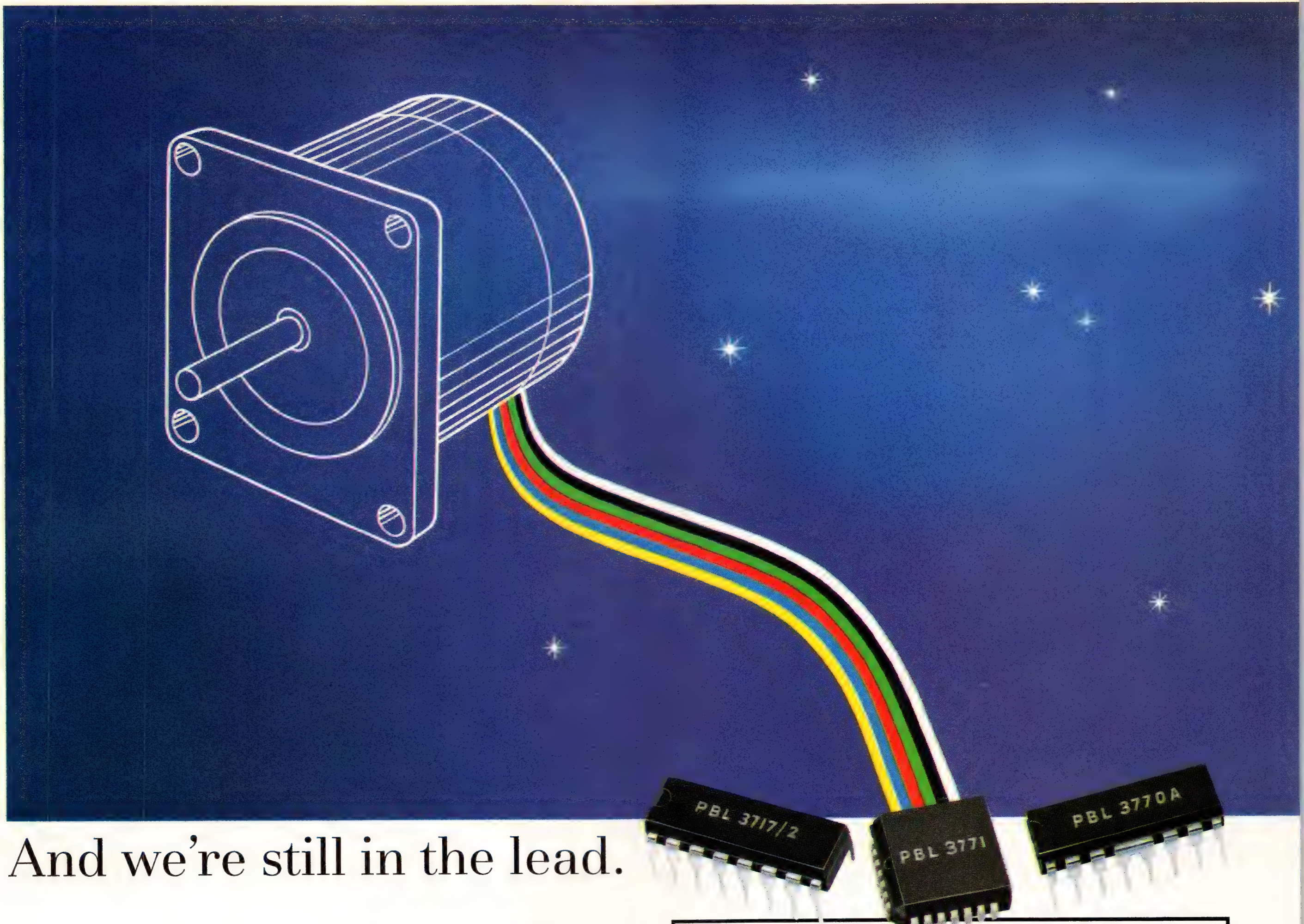

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included in resonant converters (T_2 in **Fig 1**) allows time for a converter to react to an overload before any damage occurs. The resonant tank itself is beneficial during overload situations, because it limits the rate of change of current through the transformer.

This 5V power supply is a basic implementation of resonant-mode design techniques, but it's only one of many design possibilities. Research continues in many diverse areas, including not only zero-current-switched topologies, but zero-voltage-switched topologies and a special set of third-generation topologies called "multi-resonant." CAD has been a particularly valuable research tool. The simulation ability of CAD systems gives designers valuable tools with which they can compare different topologies and optimize designs. **EDN**

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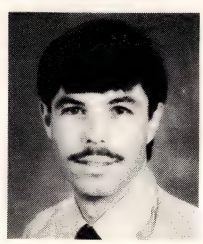
Author's biography



Frederick E Sykes is a design engineer with Gennum Corp in Burlington, Ontario, Canada, where he designs analog ICs for high-performance power-supply applications. He codesigned the first commercially available, monolithic resonant-mode controller. Fred received his B Eng in electrical and computer engineering from McMaster University in Hamilton, Ontario, Canada. In his spare time, Fred enjoys sailboarding, skiing, and computer programming.

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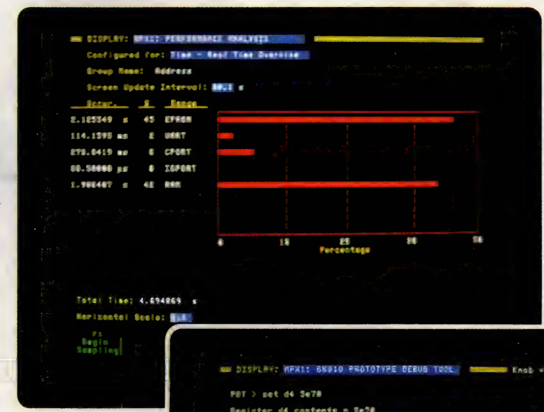

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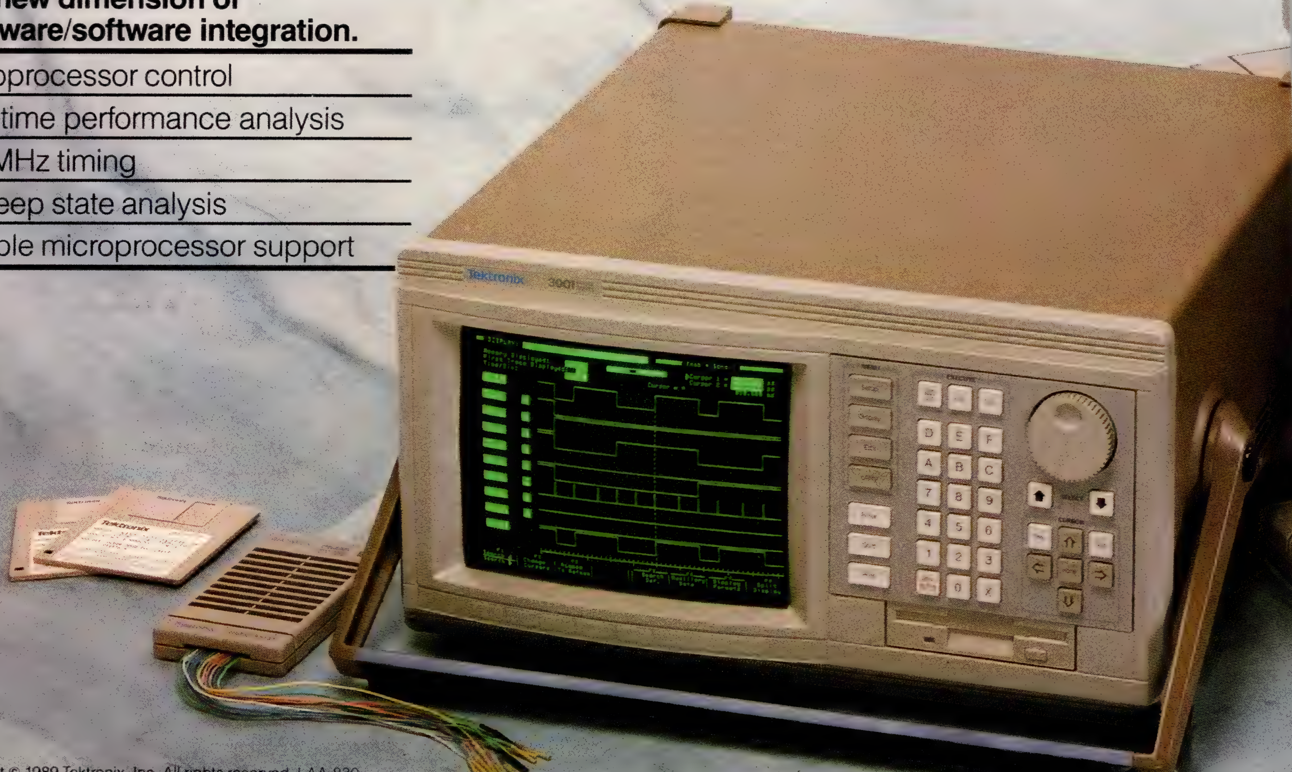

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Use real-time performance analysis to get a true, non-statistical view of system performance.

Designers of embedded control systems will especially benefit from histograms of uncompromising accuracy.

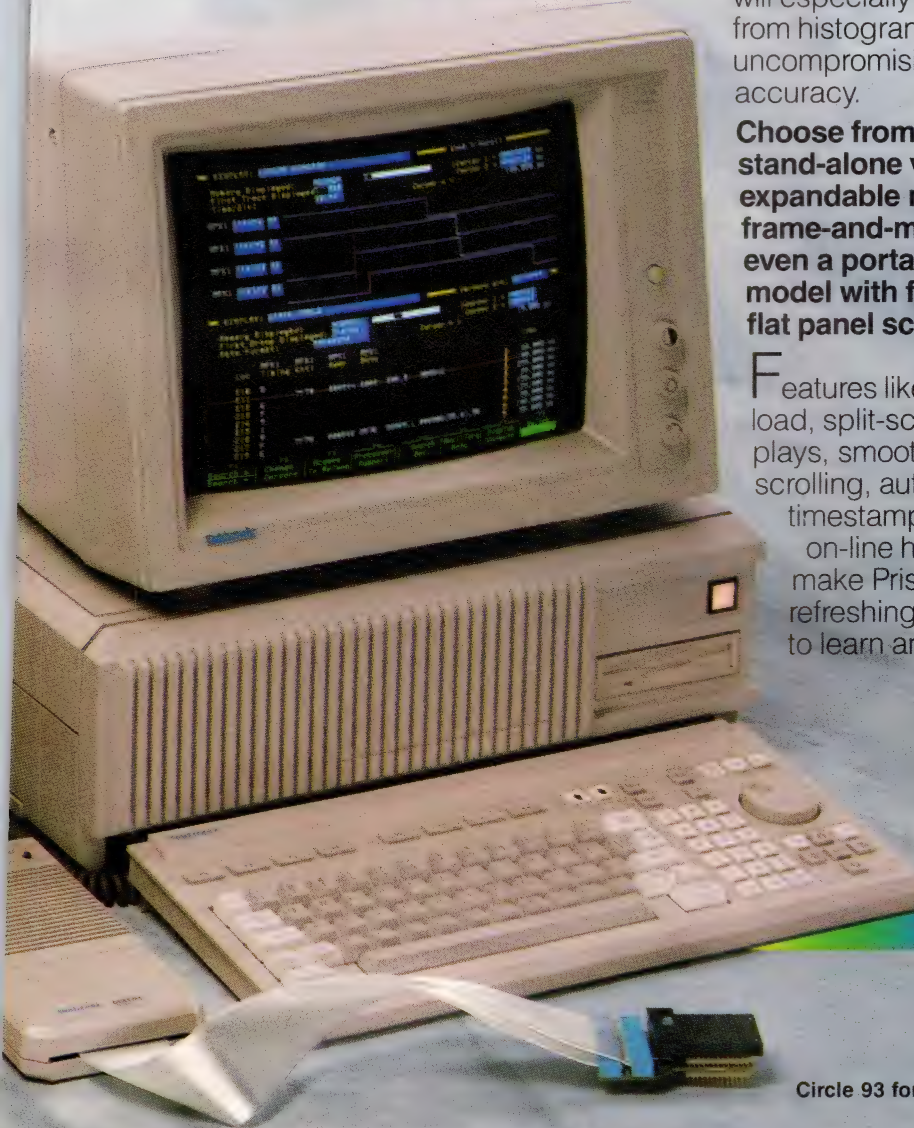
Choose from a stand-alone version, expandable mainframe-and-monitor, even a portable model with fold-up flat panel screen.

Features like autoload, split-screen displays, smooth scrolling, automatic timestamping and on-line help notes make Prism refreshingly simple to learn and use.

Complete front panel controls are included on the Prism keyboard, enabling users to move easily from one Prism mainframe to another.

The clincher? You can step into this new generation of logic analyzers at prices starting at $8600.

Call 1-800-426-2200 for our free video demo and literature packet. Prism breaks so much new ground and offers so much to build on, you owe yourself a look. For a hands-on introduction, call your Tek sales engineer soon.



Tektronix
COMMITTED TO EXCELLENCE

Circle 93 for Literature

Circle 94 for Sales Contact

Harris 80C286: C

Performance And Software - A Solid Foundation.

When you're making an architecture decision, you want proven materials and design concepts that make sense. You want dedicated support and a path for increasing your throughput. Our 80C286 provides the solid foundation and extra performance you need.

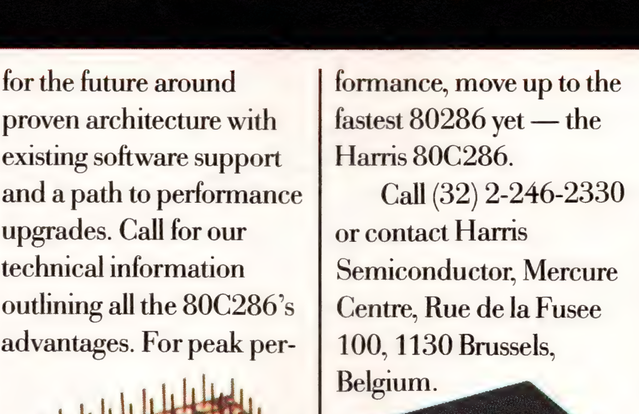
For example, our 80C286 executes 8086 and 80286 16-bit code — representing the industry's largest base of installed software — at the industry-leading speed of 25MHz. You get industry-standard software with industry-leading throughput.

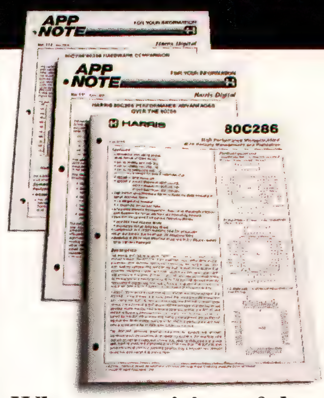
There's another key to processor selection: a growth path for the future. The 80C286 offers a wide performance range — from 12.5MHz to 16MHz through 20MHz and on to 25MHz — so you can migrate simply and smoothly when you need higher throughput.

Speed isn't the only issue, however. System requirements are becoming more and more complex with the need for multiple tasks and increased security. The 80C286 with its protected mode operation and multi-tasking capability keeps application software and data organized and secure.

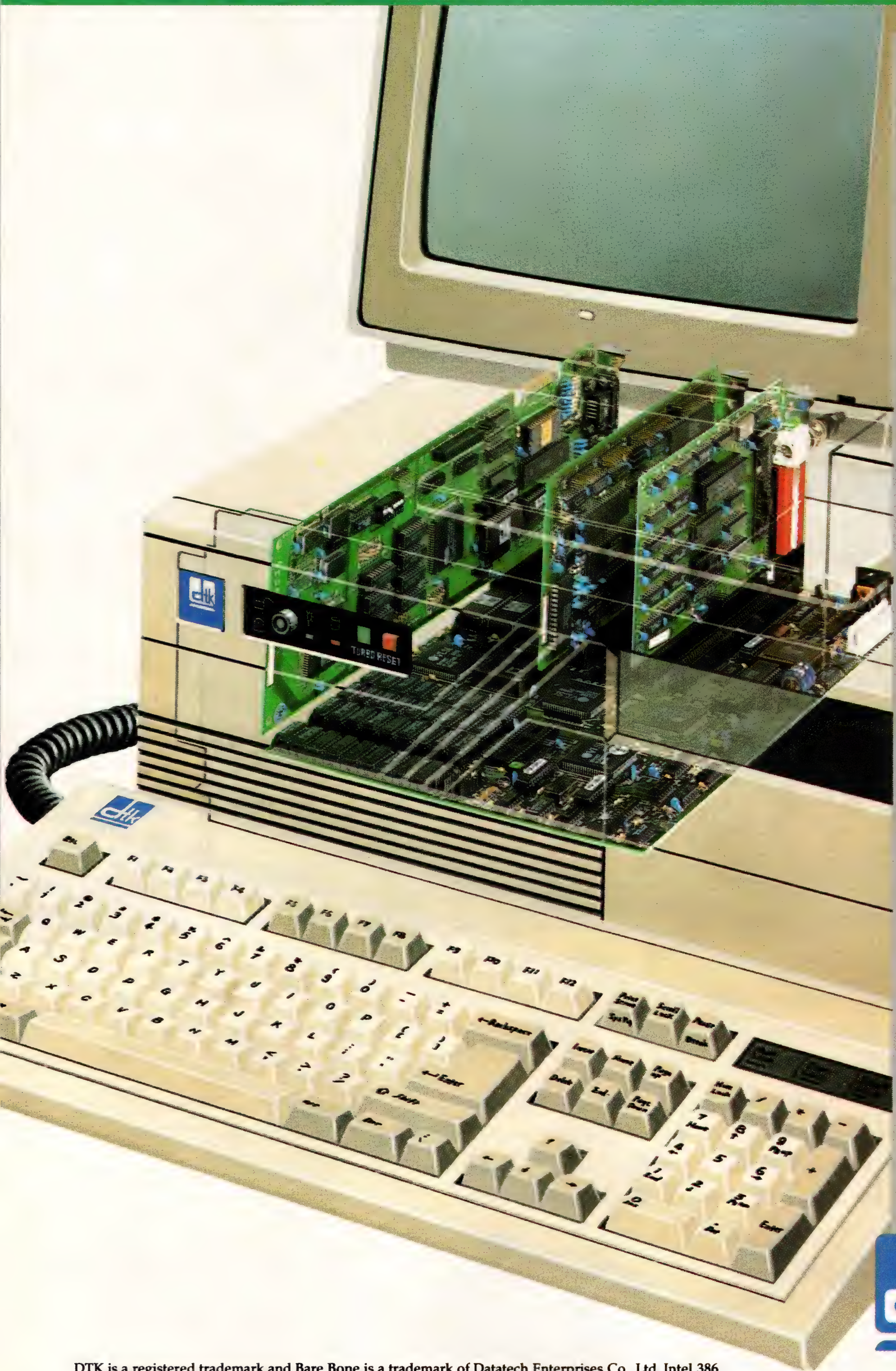
Another measure of performance is durability — running faster longer. The 80C286's low power


80C286
assic Architecture


80C286


APP NOTE
APP NOTE
HARRIS
80C286

We've got the guts, you get the glory.



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Today's sophisticated systems demand maximum compatibility and reliability. Your reputation depends on it.

DTK offers clearly superior 80386, 80286 and 8088-based Bare Bone™ systems with FCC, UL, CSA and TUV certification. Plus a wide line of motherboards that are fully compatible with AT™, XT™ and Micro Channel™ bus architectures.

They're all built to deliver the performance and reliability you need, even in rigorous manufacturing environments. We'll deliver them when you need them from our state-of-the-art 270,000 square foot manufacturing facility.

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Our inspection conforms with MIL-STD-105D, and our boards enjoy an overall reliability rate greater than 98%.

So why take chances? We've got all the guts you need at prices that are hard to beat. Go for the glory.

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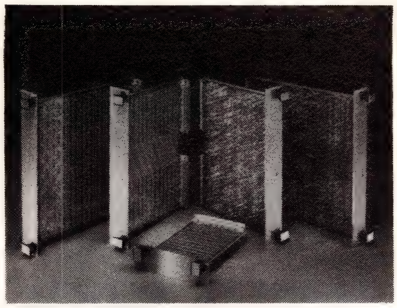
Tel: (818) 333-7533
Fax: (818) 333-5429
Ask for OEM sales.

Clearly superior.



VMEbus And Multibus II Wire-Wrap Boards

- *Have surface-mount ceramic capacitors to reduce noise*
- *Boards with pin-grid-array areas have 6-contact IC sockets*

A family of VME and Multibus II wire-wrap boards is available for one-of-a-kind and limited-production applications. The multilayer boards use surface-mount ceramic capacitors, which suppress switching noise, and axial-lead tantalum capacitors, which reduce low-frequency electrical noise. The ICs mount over the capacitors with no placement interference. Boards with pin-grid-array areas feature 6-contact IC sockets for easy insertion and reliability. All boards have double-width front panels and Scanbe E-Z-Ject ejectors. $609.

Electronic Solutions, 6790 Flanders Dr, San Diego, CA 92121. Phone (800) 854-7086; in CA, (800) 772-7086. TWX 910-335-1169.
Circle No. 366

Trackball For IBM PS/2 Computers

- *Plugs directly into the PS/2 mouse port*
- *Has two direction input buttons and a cursor drag-lock button*

The PS/2 trackball for IBM PS/2 computers is a member of the vendor's family of PC-Trac pointing devices. The unit is hardware compatible with the IBM PS/2 mouse and plugs directly into the mouse port. Its three buttons consist of two that control the X and Y directions and a third that acts as a cursor drag lock. A multiaxis-pointer driver, which comes with the trackball, continuously monitors the rate at which the pointing device is moving and provides a ballistic-gain response between 50 and 2000 pulses/in., depending on the device's velocity. The company provides a list of 40 popular pointing devices that are compatible with its driver. In addition, the software package comes with a device driver for Microsoft Windows, Windows 286, and Windows 386, and with a keyboard emulator for defining pointing-device interfaces. $119.

MicroSpeed Inc, 44000 Old Warm Springs Blvd, Fremont, CA 94538. Phone (800) 232-7888; in CA, (415) 490-1403. **Circle No. 367**

88100-Based/Workstation

- *Includes a color monitor and a 156M-byte hard-disk drive*
- *Has 8M bytes of RAM that's expandable to 32M bytes*

Based on Motorola's 88100 RISC (reduced-instruction-set computer) μP, the XD88/10 17-MIPS desktop workstation includes a color monitor, a 156M-byte hard-disk drive, and 8M bytes of RAM. The disk-drive capacity is expandable to 3G bytes and the RAM to 32M bytes. The workstation's monitor provides 1280×1024 pixel resolution, and its standard color system is expandable to 24 bit planes with an 8-bit overlay. The unit complies with the SVID (System V Interface Definition) and POSIX (Portable OS Interface) standards for Unix as well as TCP/IP (Transmission Control Protocol/Internet Protocol) for Ethernet. Because the unit also supports the company's high-speed Color≠Cache implementation of X Windows System 11.3, it runs software ported to X11 on the company's other XD88s or on 4319 68000-based workstations. The workstation also runs software written for the OnRamp graphics software library. Base unit, $15,450. Available for orders now with shipment in the first quarter of 1990.

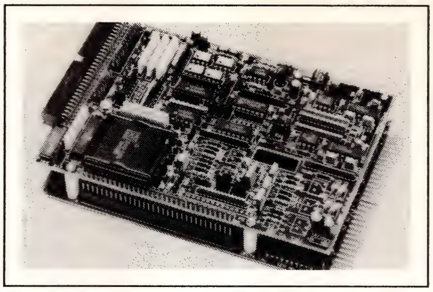
Tektronix Inc, Box 14689, Portland, OR 97214. Phone (800) 225-5434. **Circle No. 368**

STD Bus 2-Axis Motion Controller

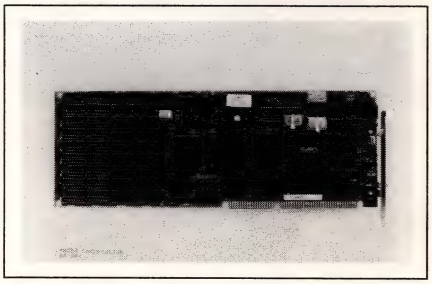
- *Contains two 40W drivers for small motors or hydraulic valves*
- *Controls 2-axis dc brush motors or a single-axis brushless motor*

Designed for 8- and 16-bit STD Bus systems, the SMCC-STD Bus motion-controller card contains two 40W drivers that are suitable for driving small motors or hydraulic valves. It can control 2-axis dc brush motors or a single-axis dc brushless motor. Phase-commutation control is provided for a 3- or 4-phase brushless dc, ac induction, or a stepper motor. The card occupies two card slots and four I/O or memory addresses, which may be selectively placed at any of 64 address locations. A custom 16-bit-internal, 8-bit-external microcontrol-

ler uses pipelining and DMA to achieve a 300-μsec servo update time. You can store motion parameters in an onboard electrically alterable ROM, which enables stand-alone operation without a host computer. Proportional, integral, and differential gains have independent velocity and acceleration feedforward terms for reducing following error to almost zero. The card employs a Basic-like programming language. $1299.



Delta Tau Data Systems, 21119 Osborne St, Canoga Park, CA 91304. Phone (818) 998-2095. FAX 818-998-7807. **Circle No. 369**



20-MHz 80286 CPU Board

- *For the passive industry-standard-architecture backplanes*
- *Has as much as 8M bytes of LIM 4.0 Expanded Memory*

The RA-804 80286 CPU board for passive ISA (industry standard architecture) backplanes contains the Phoenix BIOS in ROM, an 80287 coprocessor socket, a keyboard controller, a real-time clock, and as much as 8M bytes of LIM 4.0 expanded memory. You can install the memory in four rows of DIP sockets. Each row can handle 256k × 9-bit or 1M × 9-bit RAM chips. A daughter board accommodates four additional rows of sockets. Interleaved memory organization permits zero-wait-state operation with 80-nsec RAMs. The CPU can access the memory at a rate of 20 MHz. Because the Phoenix BIOS is in ROM, the setup routine for the expanded memory, which is part of the BIOS, is accessible without a disk drive. The unit operates from 0 to 60°C and draws 1.5A from the 5V supply. $850.

Amdex Corp, 267 Boston Rd, N Billerica, MA 01862. Phone (508) 663-2070. FAX 617-663-5094.

Circle No. 370

INTEGRATED CIRCUITS

Fuzzy-Set Comparator

- *Compares input data with known patterns*
- *Can handle eight patterns*

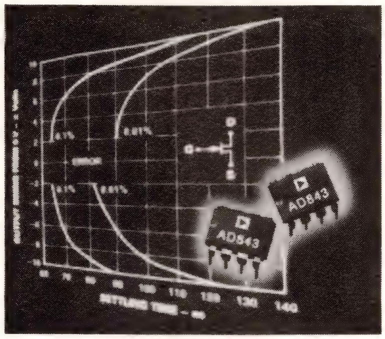
The MD1210 fuzzy-set comparator is an artificial-intelligence IC with a digital hardware neural network optimized for pattern recognition. The comparator can be taught to recognize patterns without the use of software algorithms or other preprogramming. A single chip can simultaneously compare eight unknown data streams (patterns) to one known data stream, or eight knowns to one unknown. An expansion capability lets you combine as many as 32 chips, so you can compare an input with 256 stored data patterns. The IC uses standard memory devices and contains a standard μP interface. A fuzzy-set-comparator evaluation kit is also available featuring an IBM PC/XT- and PC/AT-compatible board, which includes the MD1210, an NTSC video interface, a C-language program source on a 5¼-in. floppy disk, and a user's manual with board schematics. MD1210, $38; evaluation kit, $250.

Micro Devices, 5695B Beggs Rd, Orlando, FL 32810. Phone (407) 299-0211. **Circle No. 351**

FET-Input Op Amp

- *Has 135-nsec settling time*
- *Needs no external compensation*

The FET-input AD843 op amp, which has a gain-bandwidth product of 34 MHz, needs no external compensation to achieve its 135-nsec settling time of 10V steps to ±0.01%. The internally compensated monolithic device draws only 13 mA of quiescent current and offers a lower-cost, lower-power alternative to high-priced hybrids, which typically require external compensation and dissipate more power. In addition, the AD843's dc



characteristics benefit applications requiring high precision. The op amp's maximum input-bias current of 1 nA and its input offset voltage of 1 mV maintain low dc-offset errors. Other specs include an input offset current of 20 pA, a slew rate of 250V/μs, an open-loop gain of 30V/mV, and common-mode rejection of 76 dB. Operating from ±15V supplies, the AD843 is available in commercial-, industrial-, and military-temperature grades. Package options include 8-pin DIPs and 12-pin metal cans. From $8.80 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (508) 658-9400. TWX 710-394-6577. **Circle No. 352**

Dual Universal Switched-Capacitor Filter

- *Features three outputs*
- *Has a wide operating range*

The LMF100 switched-capacitor filter features a center-frequency operating range of 0.1 Hz to 100 kHz and a low offset voltage of 15 mV max. The LMF100 contains two second-order filters that feature three outputs each. One output performs either allpass, highpass, or notch functions; the other two outputs perform bandpass and lowpass functions. Crosstalk between the two filters exceeds −60 dB. You can tune the filter's center frequency over its entire range by selecting the ratio of external resistors and by varying the clock frequency from 5 Hz to 3.5 MHz. Clock-division ratios of 50:1 or 100:1 are pin selectable. A single LMF100 can perform a fourth-order biquadratic function or classical filter functions such as Bessel, Butterworth, Chebyshev, and elliptic. The filter operates from supply voltages of 4 to 15V or ±2 to ±7.5V. Current drain at ±5V is only 13 mA. In a 20-pin DIP, $2.50 (100).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-2273. TWX 910-339-9240. **Circle No. 353**

CMOS Military Static RAM

- *MIL-STD-883C compliant*
- *Has 64k-bit density*

The M5164 64k-bit static RAM (SRAM) is compliant with MIL-STD-883C Class B and DESC requirements. Organized as 8k×8 bits, the M5164 has access times ranging from 25 to 70 nsec. A byte-wide, 256k-bit version will be available before the end of the year. The device, which is pin compatible with many other 8k×8-bit SRAMs, is available in a 600-mil ceramic DIP and is marked with the appropriate DESC number: 5962-89691 (25 nsec) or 5962-85525 (35 to 70 nsec). From $75 (100).

Intel Corp, Box 58065, Santa Clara, CA 95052. Phone (800) 548-4725. **Circle No. 354**

Miniature DC/DC Converter

- *Has 1W output capability*
- *Has 75% min efficiency*

The NMA series of 1W dc/dc converters achieves a power density exceeding 14W/in^3. In the available SIP, the hybrid device occupies only 0.18 in.^{2} of board space. Also available is an industry-standard, 14-pin DIP. The converters provide 1W of isolated output power at effi-

ciencies between 75 and 80% from inputs of 5, 12, 24, and 48V dc. The converters are available with outputs of ±5, ±12, and ±15V dc and will operate over a temperature range of −25 to +80°C. $19.50 (1 to 9).

International Power Sources, 200 Butterfield Dr, Ashland, MA 01721. Phone (508) 881-7434. FAX 508-879-8669. TWX 510-100-3630.

Circle No. 355

CCD Driver

- *Has dual 3A outputs*
- *Achieves high contrast from CCDs*

Designed specifically to drive CCDs, the TSC430 greatly improves images in facsimile machines, copiers, and video cameras. The dual 3A-pk output driver is designed to achieve maximum contrast from CCDs. Featuring low propagation delay, the driver has a maximum skew (the crossover of the two complementary outputs) of 5 nsec. The device allows output swings between positive and negative supplies without sacrificing ac performance when driven from TTL logic. The quiescent power requirement is <5 mA at 15V. The TSC430 is available in 8-pin DIPs and a 20-pin LCC. Commercial-grade devices, from $2.75 (10,000).

Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94039. Phone (800) 888-9966; in CA, (415) 968-9241. FAX 415-967-1590. TWX 910-379-6494.

Circle No. 356

24-Pin PAL Devices

- *Delay is less than 7.5 nsec*
- *Operate at speeds to 74 MHz*

The 24-pin PAL20R8-7 family complements the company's 20-pin devices introduced in June 1988. The maximum propagation delay of the new bipolar devices is 7.5 nsec. Sustained operating frequencies of 74 MHz are obtainable under worst-case external feedback conditions. The PAL devices are supported by the company's PALASM development software and by third-party development tools. The vendor's low-cost LabPro programmer, as well as third-party programmers that have been certified by the vendor, provide programming support. The devices are available in a 24-pin, 300-mil plastic DIP and in a JEDEC-standard, 28-pin plastic leaded-chip carrier. $11.10 (1000).

Advanced Micro Devices, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400. FAX 408-982-7490.

Circle No. 357

PRESENTING THE WINNING ADVERTISEMENTS

from EDN Magazine Edition's August 3, 1989 Reader Vote Contest. Our readers evaluated the advertisements in the issue to select the ones they judged to be the most informative, helpful and attractive.

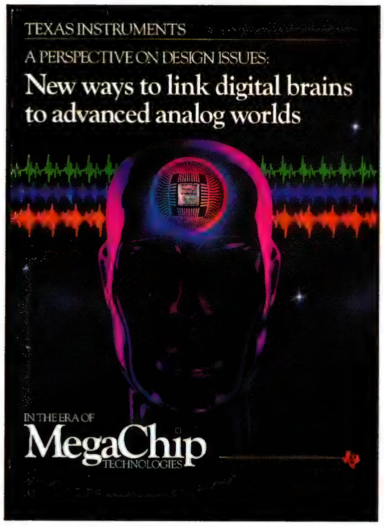
Congratulations to the advertisers and agencies who combined well-written copy and superior design to create these winning advertisements. And, a special thank you to the readers who took the time to participate.

Here then are the outstanding performers.

EDN Magazine Edition News Edition

First Place

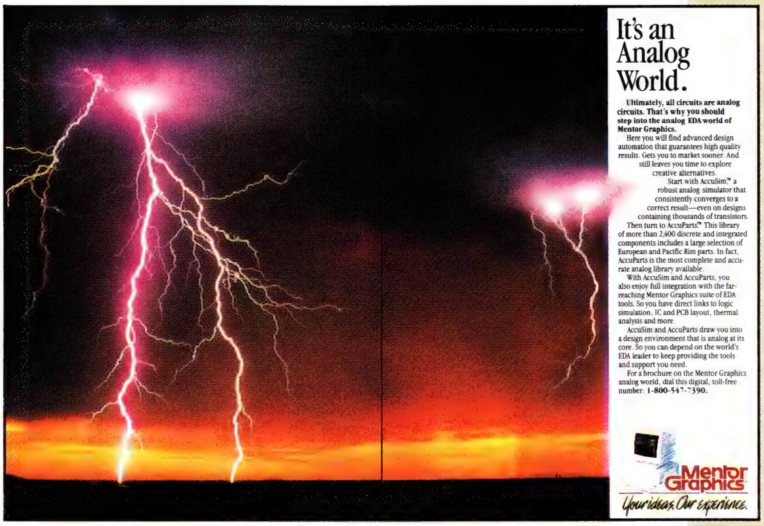
Company:
Texas Instruments
Agency:
McCann-Erickson



• "Brainy lead in graphics; well-done copy and details."
Sr. Design Engineer, Magnetic Instrumentation

• "Design caught my eye then copy gave me an education."
Systems Engineer, Electrospace Systems

• "Striking graphics!"
Design Engineer, McDonnell-Douglas



Second Place

Company:
Mentor Graphics
Agency:
KVO Advertising & Public Relations

- "Stark reality that the analog world is powerful."
  Engineer, Rockwell International

- "A real eye-catcher—brief but informative."
  Engineering Manager, Hughes Aircraft Company

- "Lightning is impressive example of analog signals."
  Sr. Engineer, Lockheed—ESC

Third Place

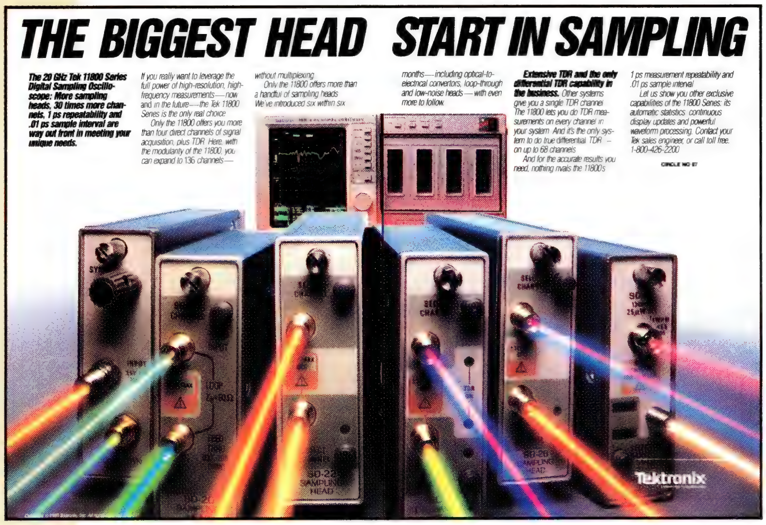
Company:
Wavetek San Diego, Inc.
Agency:
Chapman/Warwick Advertising

- "Simple analogy picture explains ease of instrument use."
  Sr. Lead Test Engineer, Honeywell MAVD

- "Clever graphic—short and to the point."
  Design Engineer, D-G Electronic Developments Co.

- "Effectively illustrates ease of operation."
  Sr. Development Engineer, Nicolet Instruments

Company:
Tektronix, Inc.
Agency:
Young & Roehr



• "Wow!"
Project Engineer, Rockwell International

• "Excellent!"
Sr. Engineer, Unisys Corporation

• "Informative and excellent taste."
Electrical Engineer, Visionetics

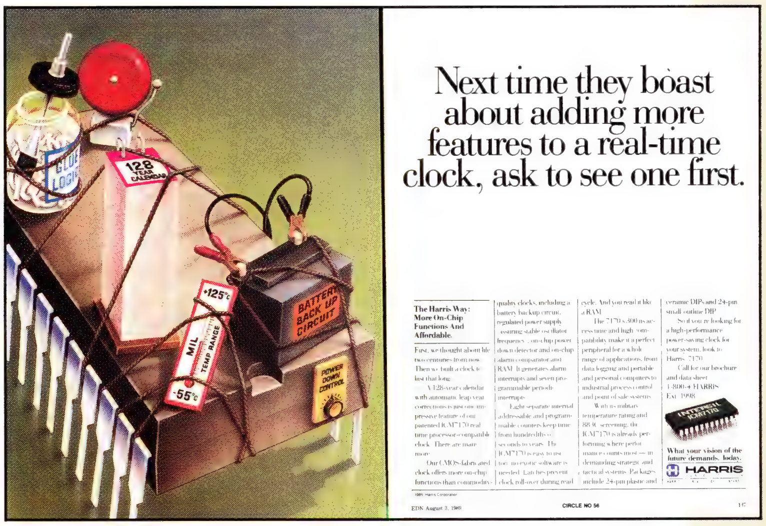
Company:
Motorola Semiconductor Products, Inc.
Agency:
Comm Ad Advertising

• "Put it together and whey have you got: a 'riscky' ad!"
Sr. Engineer, Sanders Lockheed

• "The headline says it all."
Principal Engineer, AVX Corporation

• "Informative, well laid-out, cute pun."
Project Engineer, Encore Computer Corp.

• "The graphic appeals to the engineer's mind."
Technical Engineer,
AT&T Bell Laboratories



Company:
Harris Semiconductor
Agency:
The Downs Group Inc. Advertising

• "The graphic says it all!"
Owner, Can-Tron

• "Humour always gets my attention!"
Sr. Engineer, Optronic Laboratories, Inc.

Company:
Hitachi America Ltd., Semiconductor & I.C. Division
Agency:
Sutter/Martin, Inc.

- "Provides useful information."
  Engineer, PEI Inc.

- "Eye-catching, tasteful, informative."
  President, Sycom

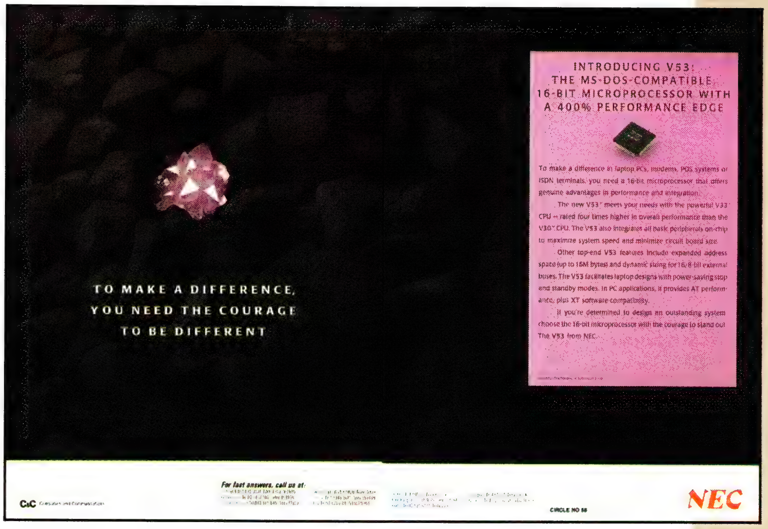
- "Terrific visual impact!"
  Senior Engineer, Eaton Corporation

Company:
TRW/LSI Products, Inc.
Agency:
Galusha & Associates

- "Modern & artistic!"
  Sr. Engineer, Ampec Corporation

- "Besides the beauty of the modern art, the ad provides concise information."
  Electrical Engineer, Johnson & Johnson

- "Concise and realistic!"
  Design Engineer, Hughes Aircraft Company



- “Artistic excellence, succinct expression.”
  Engineering Manager, BW/IP International, Inc.

- “Simple but striking graphic.”
  VP Engineering, ITS Corporation

- “Direct facts, impressive photo, not too wordy.”
  Application Engineer, Tektronix, Inc.

Company:
NEC Corporation
Agency:
Global Advertising Co., Ltd.

Company:
Rittal Corporation
Agency:
David K. Burnap Advertising Agency, Inc.

- “As a NASA employee—the picture is a real eye-catcher!”
  R&D Manager, NASA

- “Makes you feel this company’s product is really worth looking into.”
  VP Engineering, Trans Tech International

- “Space-age!”
  Technical Engineer, Rockwell International

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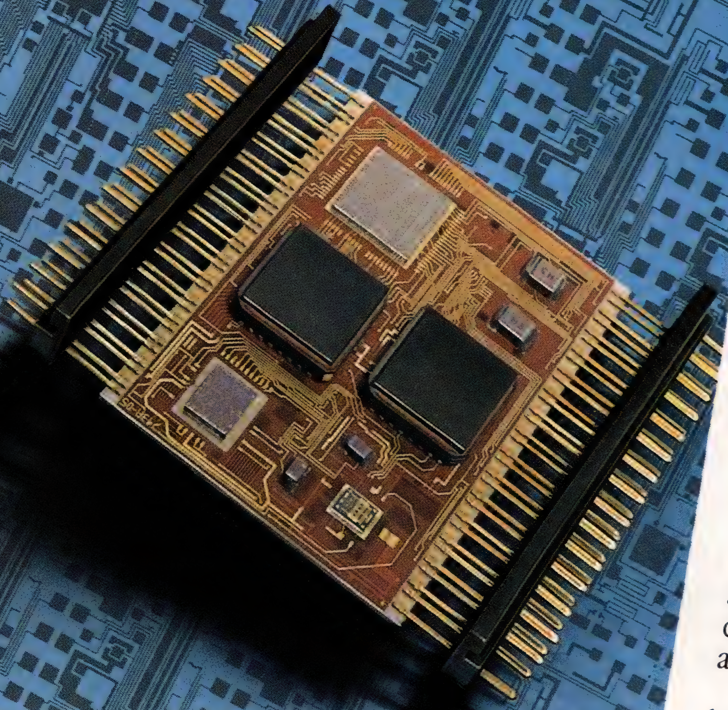
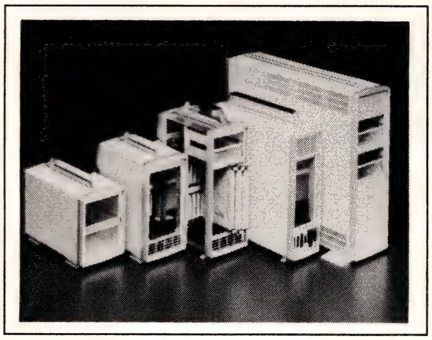


COMPONENTS & POWER SUPPLIES



Tower-Type Enclosures

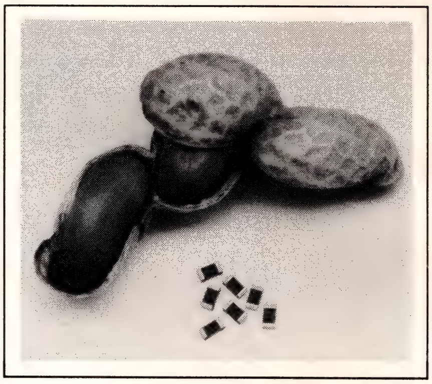
- *Available in four widths*
- *Come completely wired for VME systems*

These portable VMEbus-system enclosures come in 3U, 4U, 5U, and 6U widths. The 3U-wide units accept as many as five boards in single, double, or triple heights; the 4U and 6U enclosures accept as many as seven and 12 boards, respectively. The mechanical dimensions of all towers conform to DIN 41494, part 5. The towers measure 17 in. high and are completely wired and tested with J1 and J2 backplanes, power supplies, and fans. The units can also serve as desktop enclosures. Typical 5-slot tower, $300.

Elma Electronic Inc, 41440 Christy St, Fremont, CA 94538. Phone (415) 656-3400. FAX 415-656-3783. **Circle No. 358**

Chip Resistors

- *Available in 1206 size*
- *Offer ±0.1% accuracy*



Available in the standardized 1206 size, TNPWM thin-film chip resistors have resistance values ranging from 49.9Ω to 100 kΩ. Depending on the temperature coefficient desired (±25 ppm°C, Characteristic E or ±50 ppm/°C, Characteristic H), the resistors are available with tolerances of ±0.1, 1, 2, or 5%. Minimum resistance values for ±0.1% tolerance units is 100Ω. The resistors have flow-solderable, wraparound terminations that enhance automatic-placement capabilities. A

nickel-barrier coating provides extra protection for the inner electrode. The units are available in 8-mm tape and reel, tray, or bulk packaging. Units with 25-ppm/°C temperature coefficient and ±0.1% tolerance, $2.71 (1000). Delivery, stock to 11 weeks ARO.

Dale Electronics Inc, 1122 23rd St, Columbus, NE 68601. Phone (402) 371-0080. **Circle No. 359**

Voltage-Controlled Oscillators

- *Operate from a single supply*
- *Have a 5-MHz/V tuning sensitivity*

D-1000 Series voltage-controlled oscillators cover a 1000- to 2000-MHz range with a phase-noise characteristic of −95, −105, and −120 dBc/Hz at offsets of 1, 5, and 25 kHz, respectively. They have a ±10-MHz tuning range and tune from 0 to 15V dc with a sensitivity of 5 MHz/V. The units have a buffered output of 10±2 dBm and draw 40 mA from a 12V supply. Harmonic suppression equals −15 dBc. Frequency pulling and pushing equals 500 kHz and 1 MHz, respectively. Completely enclosed in a metal package, the oscillators operate over a 0 to 70°C range. $130.

Z-Communications Inc, 5450 NW 33rd Ave, Fort Lauderdale, FL 33309. Phone (305) 735-1000. FAX (305) 735-1094. **Circle No. 360**

EMI Filter Module

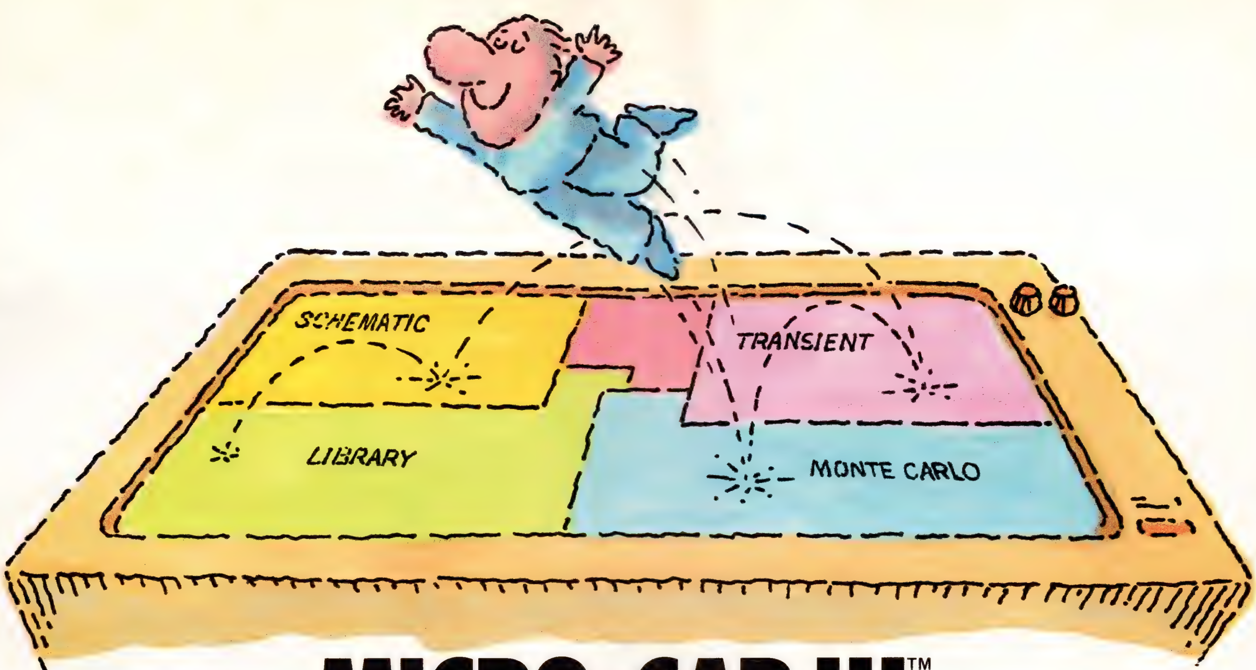
- *Operates to 300 MHz*
- *Works with RS-232C signals*

This filter module provides a convenient way for designers to eliminate the problems of stray EMI in signal cables. The module has two DB-25-type connectors (1 male and

1 female) and plugs between an RS-232C cable and an input or output port. Common-mode magnetics filter all lines except the frame ground (pin 1). The filter can attenuate EMI by at least 15 dB over the critical 30- to 300-MHz range and have no effect on the data signals. $29.95.

Coilcraft, 1102 Silver Lake Rd, Cary, IL 60013. Phone (708) 639-6400. **Circle No. 361**

TURN TO PAGE 264



MICRO-CAP III.™ THIRD-GENERATION INTERACTIVE CIRCUIT ANALYSIS. MORE POWER. MORE SPEED. LESS WORK.

MICRO-CAP III,™ the third generation of the top selling IBM® PC-based interactive CAE tool, adds even more accuracy, speed, and simplicity to circuit design and simulation.

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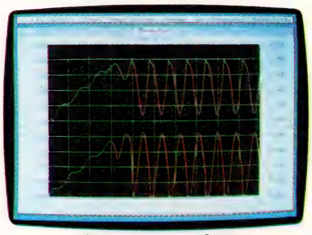
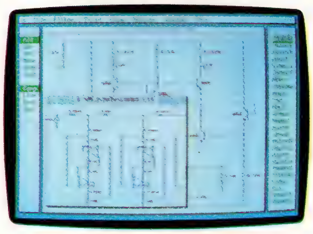
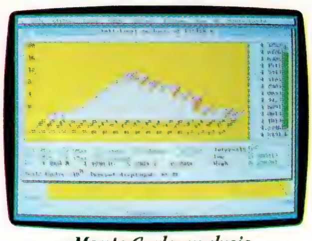
We've added routines for noise, impedance and conductance—even Monte Carlo routines for statistical analysis of production yield. Plus algebraic formula parsers for plotting almost any desired function.



Transient analysis



Schematic editor



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CIRCLE NO 99

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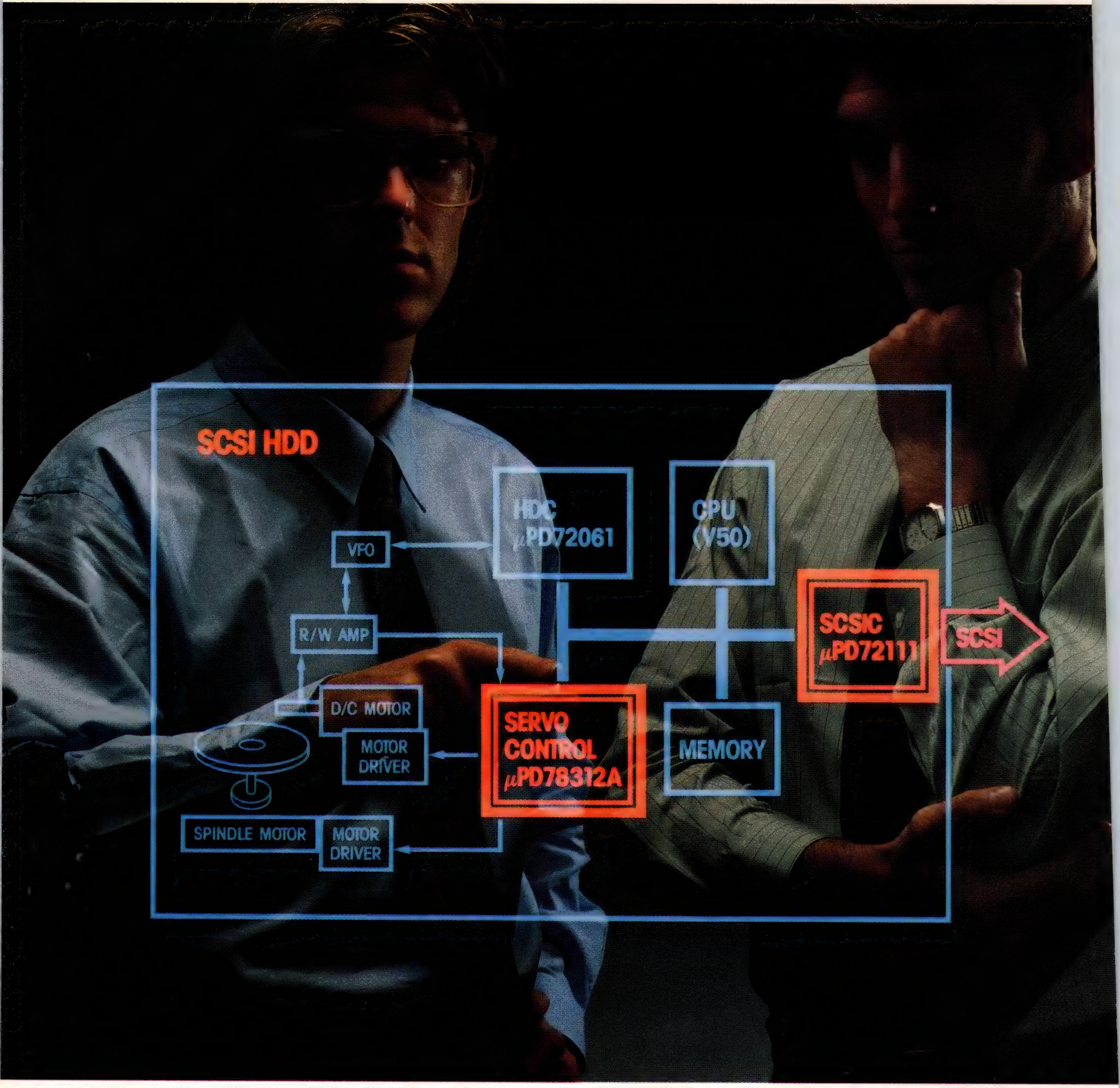

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NEC's 16-bit singlechip microcontroller excels in interrupt response. The μPD78312A incorporates 8-level priority interrupt. It also gives you two exclusive hardware interrupt handling features that reduce software overhead.

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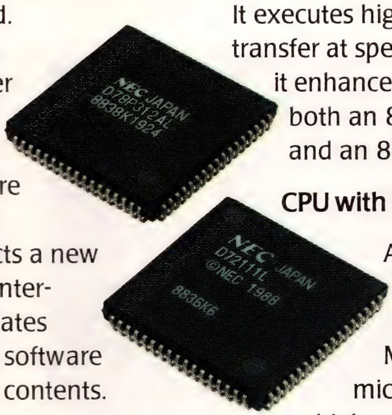
- ☐ Context Switching selects a new register bank for each interrupt request and eliminates the need for additional software to save current register contents.



The μPD78312A offers all basic peripheral functions on-chip to simplify your design and minimize circuit board size.

- ☐ 2-channel, 16-bit up/down counter with quadruple counting and up/down discrimination.
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- ☐ EPROM version available.

Versatile, high-speed SCSI controller.

Our SCSI controller gives you a competitive edge with features like high-speed sequence control. Overhead is minimized because high-level commands drive an on-chip, hard-wired sequencer.

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CPU with high-speed DMA controller.

As host to the SCSI controller, our chip set provides the V50™, a powerful, MS-DOS-compatible, 16-bit microprocessor. It features a high-speed, on-chip DMA controller capable of data transfer rates up to 2.5M words/sec at 10MHz.

If you want clear solutions to the challenges of hard disk drive design, call NEC. Our experts have been driving the technology for years.

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CIRCLE NO 103

CAE & SOFTWARE DEVELOPMENT TOOLS

Enhanced Design Tool For Gate Arrays

- *Provides automatic placement and routing features*
- *Balances clock loads to minimize skew*

Action Logic System (ALS) version 1.2 is an enhanced tool for integrating logic functions into the vendor's Act1 family of field-programmable gate arrays. The system runs on Apollo, Sun, or 80386-based workstations and is compatible with Mentor, Valid, Viewlogic, and OrCAD CAE schematic-capture and simulation tools. ALS performs fully automatic 100% placement and routing, even when gate utilization is as high as 95%. The improvements to the placement algorithms include four levels of critical-net assignment and automatic balancing of clock loads. The clock-balancing algorithms minimize clock skew and allow you to predict the postroute performance of the chip. Other improvements include a new validator; an electrical-rules checker that informs you of the routability of your design and offers suggestions for improvement; and a timing analyzer that can analyze asynchronous loops. From $9950 for the OrCAD/PC 386 version.

Actel Corp, Actel Inquiry Processing, Code ALB025, Box 2813, Torrance, CA 90509. Phone (408) 739-1010. FAX 408-739-1540.

Circle No. 362

Cross-Debugger For 80386

- *Aids software design for embedded systems*
- *Runs on VAX machines under the VMS operating system*

The DB-386 cross-debugger allows software-development engineers who use VAX/VMS computers to debug software that will run on 80386-based embedded systems. The debugger offers interactive source-level debugging capabilities for programs written in Intel's C-386, PL/M-386, Fortran-386, or ASM-386, or in any mix of these languages. It provides a simulated real-time 80386 environment that includes simulation of the 80386 CPU, 80387 numeric coprocessor, 8259A programmable interrupt controller, and 8254 programmable interval timer. You can therefore develop and debug your software before the target hardware system is complete. A complete development package includes the VMS ASM-386 macroassembler, the VMS RLL-386 utilities for linking and tracking software modules, the VMS DB-386 debugger, and a choice of one compiler (VMS C-386,

PL/M-386, or Fortran-386). $14,000 for MicroVAX systems; $18,000 for VAX systems.

Intel Corp, Box 58065, Santa Clara, CA 95052. Phone (800) 874-6835. **Circle No. 363**

Fortran For FlexOS 386

- *Provides extensions to the Fortran-77 standard*
- *Generates protected-mode code for the 80386 processor*

Lahey F77L-386 for FlexOS is a complete implementation of the ANSI X3.9-1978 Fortran-77 standard, but it also provides some extensions that increase the utility of the language under FlexOS 386. The compiler generates protected-mode code for the 80386 µP, allows programs to address as many as 4G bytes of memory, and permits interprocess communication by means of pipes. In addition, the compiler can generate output in Unix COFF (Common Object File Format) files and provide extensive error reporting. Because FlexOS 386 is compatible with MS-DOS 3.3 media and allows you to run DOS 3.3 in a separate partition of memory, you'll be able to continue using your MS/PC-DOS applications. $977.

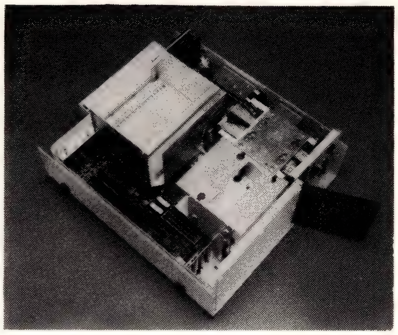
TransWare Enterprises Inc, 5091 Durango Ct, San Jose, CA 95118. Phone (408) 723-2102. **Circle No. 364**

Debugger For OS/2

- *Works with several high-level languages*
- *Allows both runtime and postmortem debugging*

MultiScope is a multilanguage debugger compatible with any language compiler that generates standard CodeView OS/2 debugging information. Such languages currently include the vendor's Modula OS/2, Microsoft C, and IBM C/2. The debugger can work in either the OS/2 text mode or in the Presentation Manager mode. It allows both runtime and postmortem debugging and can debug threads, dynamic-link libraries, and child processes. The postmortem debugging feature can capture the program-execution state of an application that was running outside the debugger at the time of a crash; you can examine the resulting dump to find the state of the program when it crashed. MultiScope provides as many as 13 program views simultaneously, as well as graphical data-structure display. The user interface features pop-up menus and single-key commands. $299.

Logitech Inc, 6505 Kaiser Dr, Fremont, CA 94555. Phone (415) 795-8500. FAX 415-792-8901. **Circle No. 365**



Industrial PC For Data Acquisition

- *Contains cage for signal-conditioning cards*
- *Offers many mounting and customization options*

The VIPc is an 80286-based computer packaged for industrial data acquisition. The small mother board, which contains one 8-bit and three 16-bit expansion slots, can accommodate 4M bytes of RAM. Within the unit is space for a cage that can hold as many as 10 signal-conditioning boards packaged as 3U-size Eurocards. For security, and to keep out foreign material, the optional floppy-disk drive is concealed behind a hinged cover. The unit mounts on a benchtop or in a standard 19-in. equipment rack. You can also surface mount it with the 19-in. dimension positioned vertically or attach a carrying handle. For customization, you can use the space available on flat, removable plates to add connectors of your choice and such items as a small flat-panel display. You can plug data-acquisition boards called "carriers" into the PC bus slots and you can plug additional modules onto these carriers. From $3995.

Burr-Brown Corp, 1141 W Grant Rd, MS 131, Tucson, AZ 85705. Phone (602) 746-1111. FAX 602-623-8965. **Circle No. 373**

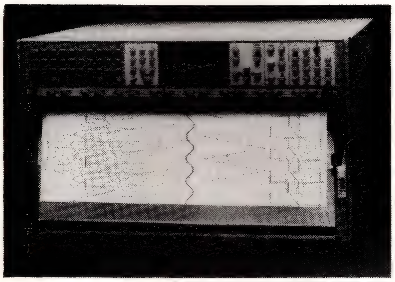
PC-Based Logic Analyzers

- *Accept 32 inputs*
- *Capture 4-channel timing data at 100 MHz*

The ID161 is a logic analyzer on a single PC bus card. You can configure it with 32 inputs and use it as a state analyzer for 8-bit μPs. When you operate it in multiplexed mode with four channels, it can acquire timing data at 100 MHz. The ID160 is a similar unit but has a top speed of 50 MHz. Complex trigger capabilities facilitate using the boards

as debugging tools. Among those capabilities are multilevel triggering, pass counting, event timing, event counting, and selective data capture. The software that accompanies the units lets you write test programs in a simple language and analyze software performance by constructing histograms. ID161, $895; ID160, $695.

Innotec Design Inc, 4878 Embassy Circle, La Palma, CA 90623. Phone (714) 527-8540. FAX 714-527-1812. **Circle No. 374**



Thermal-Array Recorder

- *Can record 24-channel data*
- *Provides 35-kHz bandwidth*

The TA4000 recorder uses one stationary thermal array to reproduce as many as 24 channels of analog data on 15-in.-wide paper. Any trace can occupy a portion of the chart or the full chart width. Because the unit uses a single print head, full-width traces do not have gaps running down the chart as do those reproduced by recorders that use multiple arrays. The recorder displays signals with 10-kHz bandwidth in real time and, by storing 128,000,000 data samples/channel, allows capture and subsequent display of 35-kHz data. There is no parallax because the unit prints grids along with the data. From $14,300 (for an 8-channel system with nine event markers and annotation capability). Delivery, four to six weeks ARO.

Gould Inc, 3631 Perkins Ave, Cleveland, OH 44114. Phone (800) 321-3029; in OH, (216) 361-3315. FAX 216-881-4256. **Circle No. 375**

50/100-MHz, 240-Channel State/Timing Analyzer

- *Uses keyboard for command entry*
- *Includes two $3^1/_2$-in. floppy-disk drives*

The 5500, a logic analyzer intended to meet the needs of most users, can include from 48 to 240 channels that perform state or timing analysis at 50 MHz. The 50-MHz state-analysis capability is more than adequate for the fastest 32-bit processors currently available. Through multiplexing, which halves the number of channels, the instrument can perform timing analysis to 100 MHz. The self-contained unit includes a command-entry keyboard, whose layout is similar to that of an IBM PC keyboard, and a pair of 3½-in. floppy-disk drives. You can store setup information as well as data on disk. The unit stores 12k samples/channel at 100 MHz, captures 4-nsec glitches, and time-stamps unrelated samples with 10-nsec resolution. The triggering has 14 decision levels. $16,500 with 48 channels.

Marconi Instruments Inc, 7570 E Redfield Rd, Scottsdale, AZ 85260. Phone (800) 223-4143; in AZ, (602) 998-9294. FAX 602-998-9112.
Circle No. 378

State/Timing Analyzer That Samples To 2 GHz

- *Accepts as many as 256 inputs*
- *Can include IBM PC/AT-compatible computer*

You can purchase logic analyzers in the KLA/2 family with and without an integral IBM PC/AT-compatible computer. The modular system allows you to choose input modules with varying speeds and channel capacities. The portable system can house four modules; the tower and rack-mountable configurations each can house six modules. The general-purpose GPDA module has 96 channels usable for state or timing analysis at 100 MHz. By multiplexing, the speed increases to 200 MHz, though the channel capacity is halved. You can equip the GPDA with 4k or 16k bits of memory per channel. As a timing analyzer, the GPDA uses transitional timing to increase its effective memory depth. The VHSTA (very-high-speed timing analyzer) module allows 1-GHz data acquisition on 16 channels or 2-GHz acquisition on eight channels. Mainframes, $14,995; modules, $15,995. Delivery, 10 weeks ARO.

Kontron Electronics Inc, 630 Clyde Ave, Mountain View, CA 94039. Phone (800) 227-8834; in CA, (415) 965-7020. FAX 415-965-3505.
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32-BIT	80386, 68020 (25 MHZ)

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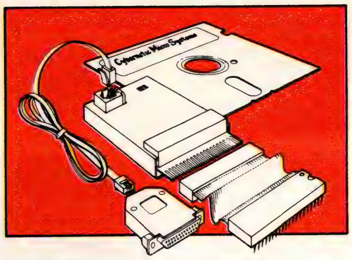

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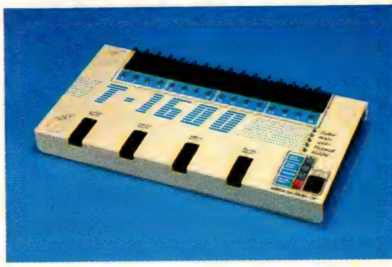

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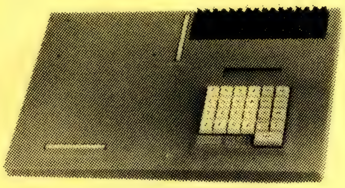

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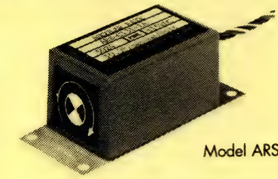

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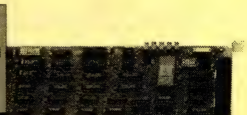

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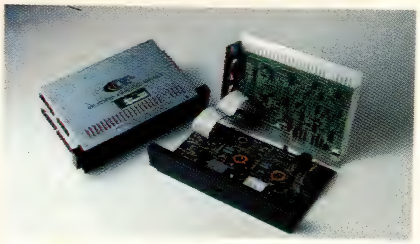

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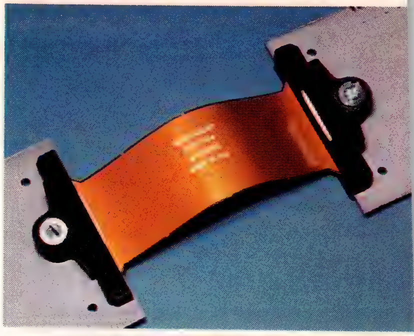

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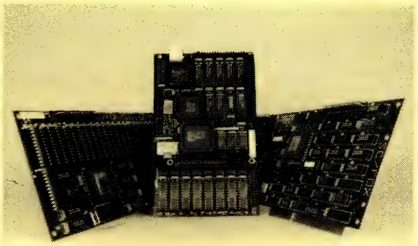

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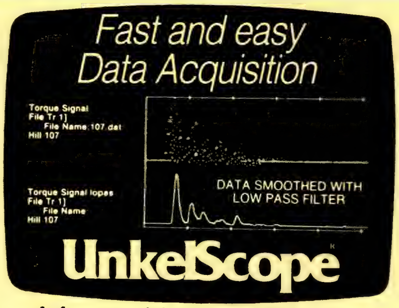

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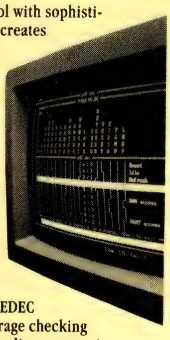

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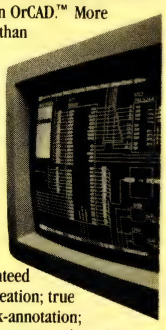

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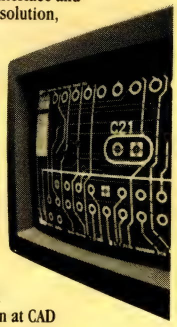

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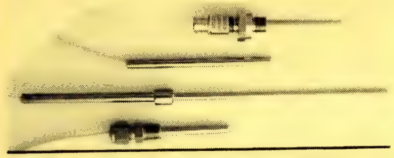

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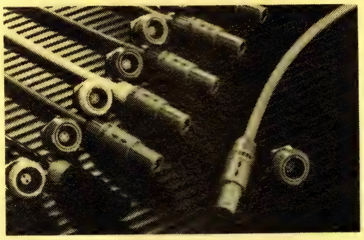

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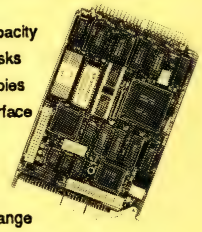

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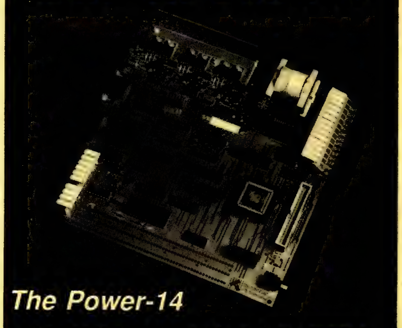

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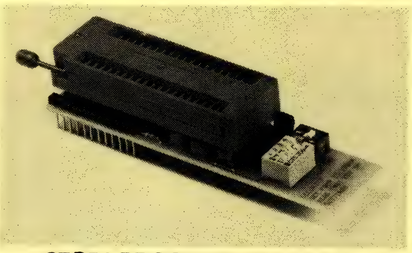

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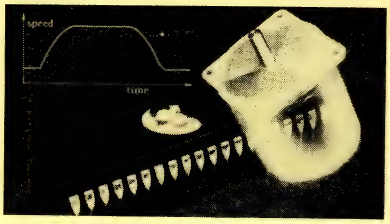

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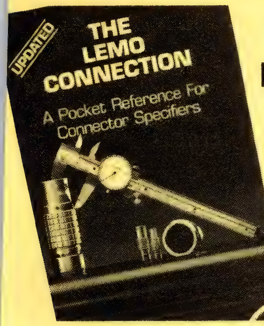

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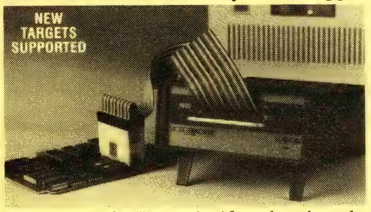

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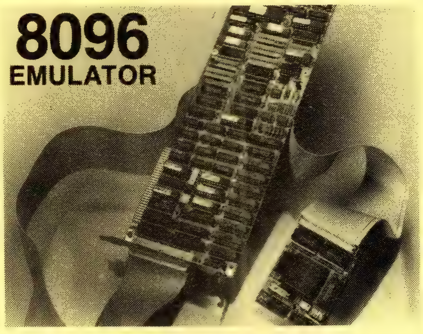

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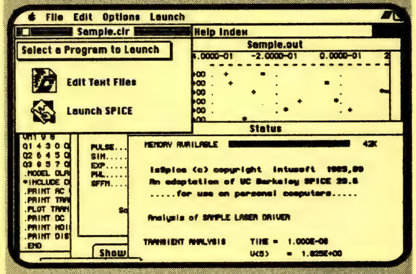

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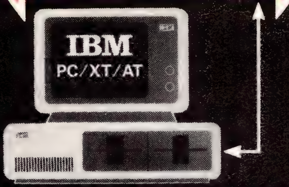

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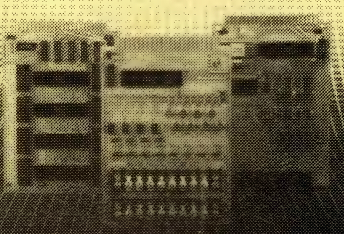

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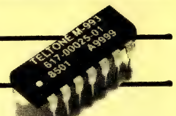

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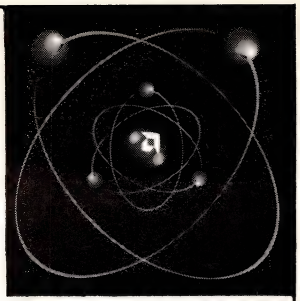

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Must possess PhD EE/MSEE or related sciences degree. Requires 8 years direct wafer fab experience with 5 years supervisory background. Must be familiar with photo, thin films, etch and diffusion. Understanding of devices and product analysis and reliability issues a must.

Section Manager—Product Engineering
MS/BSEE-Chemical Engineering or Physics. Requires 5-7 years experience with process/product engineering supporting our state-of-the-art wafer fabs. Must be familiar with CMOS/ NMOS products.

Product Engineers
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BS/MS with 3+ years transfer double-level metal process, characterization, modeling process/transistors. Will develop process cross-sectional flows, parametric targets. (Days & 2nd shift available).

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BS/EE, Physics or Chemistry required. Diffusion/CVD experience required. Knowledge of SPC and process characterization is a plus.

Sr. Process Engineer
Must have hands-on experience with plasma etch, polysilicon, nitride, silicide, metals and oxide, as well as ability to install new etchers, process integration, SPC/SQC, process transfer. Familiarity with submicron plasma etch process a plus.

Sr. Process Engineer
BS/MS EE or Chemical Engineering required. Experience in photo sustaining, positive photoresist process experience, SPC, 5X steppers or IX PE scanners. Process work with new transfer of one micron and submicron technologies required. Must be available for off shift.

Sr. Facilities Engineer
HVAC background required with piping, clean room and 4 years experience in a semiconductor atmosphere. BS ME required.

Process Engineer—Photo (or) Etch
BS/MS with 2+ years experience. Will sustain processes on off-shift. Familiarity with steppers (GCA, ASM, P&E or 500/600). Prefer AME, LAM or Tegal etchers.

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Sr. Process Engineer
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Equipment Maintenance Technicians
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You'll need experience in the mechanical design of satellite communication antennas, including expertise in composites for reflectors/feed tower structures, feed network layouts and RF components. A background in computerized mechanical/thermal analysis techniques is desired.

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You'll design spacecraft antenna systems including multiple and shaped-beams as well as feed arrays, networks and reflectors. Interfacing with electrical and mechanical design teams, you'll analyze antenna performance while participating in project reviews.

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You'll need at least 3 years experience in the integration, test verification and launching of spacecraft. Developing test plans and procedures, you'll define hardware requirements and evaluate test results. You must possess familiarity with spacecraft systems, software, mechanisms, power and/or communications sub-systems.

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Several opportunities exist for Communications Systems Engineers to perform system engineering duties including generation of specs and test requirements, I&T support, and launch/mission operations. A minimum of 3 years experience is required. Opportunities exist for:

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Spacecraft Power Systems

You'll need to be familiar with battery and solar array technologies and power regulation topologies as well as possess demonstrated analytical skills enabling you to synthesize space power system requirements from mission requirements.

Spacecraft Power Electronics

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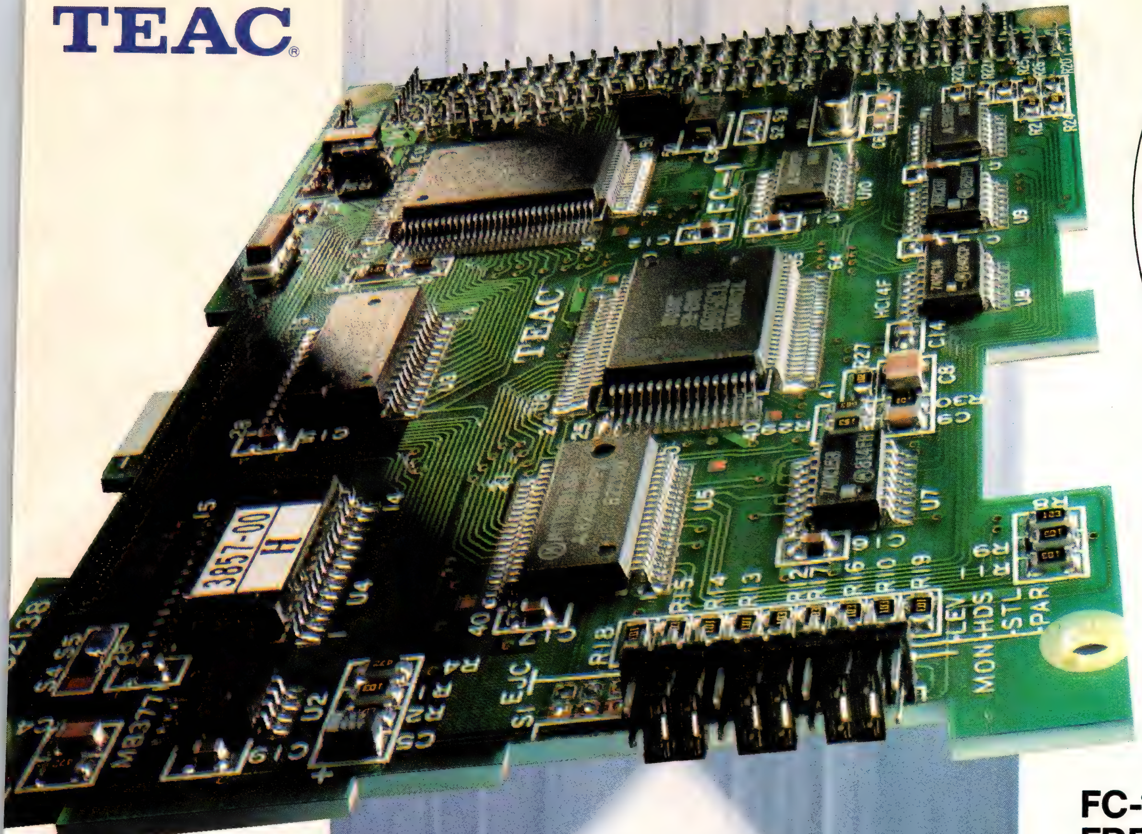

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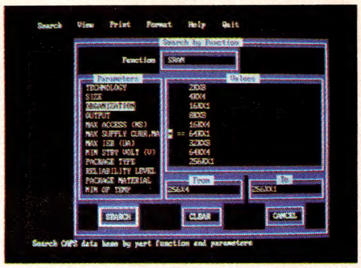
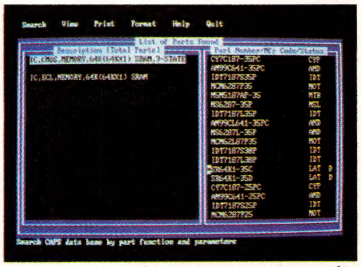


CAPS/IC searches IC-memory components to find 64k SRAMs.



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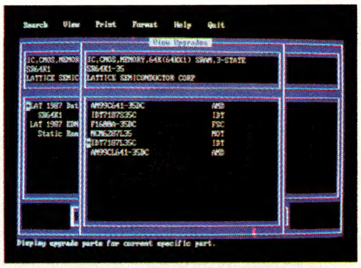

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